Digitally Intensive Sub-Sampling Mixer-First RF Front-End Architectures in 1.2 V, 65 nm CMOS

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By

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(17PHPE03)

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DECLARATION

I hereby declare that the matter embodied in this thesis titled **"Digitally Intensive Sub-Sampling Mixer-First RF Front-End Architectures in 1.2 V, 65 nm CMOS"** submitted to the University of Hyderabad for the award of Doctor of Philosophy in Electronics Science and Engineering is a record of original research work carried out by me under the supervision of Dr. Vijay Shankar Pasupureddi and Prof. M. Ghanashyam Krishna, Center for Advanced Studies in Electronics Science and Technology (CASEST), School of Physics, University of Hyderabad. To the best of my knowledge, the thesis is not submitted for any degree in any University or institute.

Date: 26-06-2023

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CERTIFICATE

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This is to certify that the thesis entitled **"Digitally Intensive Sub-Sampling Mixer-First RF Front-End Architectures in 1.2 V, 65 nm CMOS"** submitted by **Mr. Rakesh Varma Rena** bearing registration number 17PHPE03 in partial fulfilment of the requirements for the award of **Doctor of Philosophy** in Center for Advanced Studies in Electronics Science and Technology (CASEST), School of Physics is a bonafide work carried out by her under my supervision and guidance.

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Journal publications:

1. **Rakesh Varma Rena**, Raviteja Kammari, Vijay Shankar P., "0.4-1GHz Sub-sampling Mixer-First RF Front-End with 50dB HR3, +10dBm IB-IIP3 in 65nm CMOS", in IEEE Transactions On Very Large Scale Integration (VLSI) Systems, DOI: 10.1109/TVLSI.2023.3269011.
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GHz, 90 MHz BW, 4.7 dB NF quarter-rate sub-sampling mixer-first direct down-conversion RF front-end ", is submitted to IEEE Transactions On Very Large Scale Integration (VLSI) Systems(under review).

Conference proceedings:

1. **Rakesh Rena**, Suraj Kumar Verma and Vijaya Sankara Rao Pasupureddi, "A Process Scalable Architecture for Low Noise Figure Sub-Sampling Mixer-First RF Front-End," 2021 IEEE International Symposium on Circuits and Systems (ISCAS), 2021, pp. 1-5, doi: 10.1109/ISCAS51556.2021.9401387.
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Dedicated

To my parents

Lalitha Rena and Narsaiah Rena

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Abstract

To meet the ever-growing need for connected devices, advanced wireless systems have to accommodate tens of billions of wireless devices to support a wide range of applications in various communication standards. The wireless communication standards such as IEEE 802.15.4-2020 are designed to provide better coverage for low-cost, portable wireless systems with limited power consumption for various applications such as smart utility networks(SUN), rail communications and control(RCC), healthcare and industrial monitoring. These applications operate in multiple bands over a wide frequency range from 0.16 GHz to 2.4 GHz and have low data rates; hence, they should consume low power for long battery life. To meet these requirements, the receiver's RF front-end must be re-configurable, and power consumption needs to be low while maintaining the sensitivity of the receiver. The mixer-first RF front-end architecture operates over a wide range of frequencies by tuning its local oscillator frequency or sampling frequency(f_s). Therefore, a single mixer-first RF front-end is sufficient to cover complete or most of the sub-2.4 GHz IEEE 802.15.4e standard applications.

The mixer-first receivers employ N-path mixers and filters, which are excited by non-overlapping clock phases and hence require clock dividers to generate precise multi-phase non-overlapping clocks. These dividers require a reference clock frequency of $Nf_s/2$ for generating non-overlapping clocks with a frequency, f_s. In RF sampling-based mixer-first RF front-ends requires a sampling frequency greater than or equal to f_s, which increases the power consumption of these non-overlapping clock generation and distribution circuitry increases with the increasing f_s. In addition, the stringent jitter requirements increase the power consumption of the frequency synthesizers at high frequencies. Hence, the power consumption of the clock generation circuit is no longer negligible since it increases with the input RF frequency, f_{RF}. On the other hand, the sub-sampling down-conversion requires a low clock frequency and hence reduces the power consumption of non-overlapping clock generation, distribution circuits, and frequency synthesizer. However, the sub-sampling down-conversion has not been employed in mixer-first receiver RF front-ends due to the disadvantage of high noise figure from inherent noise folding and lack of RF port impedance matching because of non-zero IF down-conversion. Therefore, the main focus of this thesis

is to design digitally intensive sub-sampling mixer-first RF front-ends.

To address these issues, the first half of the thesis focuses on developing a sub-sampling multi-path down-conversion mixer scheme to reject the harmonic down-conversion to odd multiples of $f_s/4$, thereby alleviating the effect of noise folding and leading to a low noise figure.In addition, an IF stage impedance matching scheme is proposed that provides a 50 Ω impedance at the RF port of the mixer using an IF stage M-phase switch-capacitor band-pass filter connected in shunt at the input of the IF-LNA. Therefore, by employing these two schemes, a first of its kind process scalable low noise figure highly linear sub-sampling mixer-first RF front-end is proposed in this work. However, this work is also a non-zero IF down-conversion which is heterodyne in nature, and hence the passive mixer transparency property can not be exploited without the need for an additional circuit at the IF, such as M-phase filter for providing impedance matching at the RF port by impedance translation. To address this issue, a unique feature of sub-sampling, i.e. quarter-rate sub-sampling, is exploited, and a direct down-conversion scheme is proposed in this work.

The second part of the thesis presents the above mentioned concept of a quarter-rate sub-sampling direct down-conversion scheme using a sampling frequency at least three times lower than the input RF frequency and a harmonic re-combination scheme for achieving direct down-conversion using the third harmonic of f_s. The proposed RF front-end simultaneously achieves quadrature direct down-conversion and impedance matching by using the third harmonic of the quarter-rate sub-sampling frequency, f_s. This way, the quarter-rate sub-sampling direct down-conversion scheme saves the power consumption of non-overlapping clock generation, distribution circuits, and frequency synthesizer than the traditional RF sampling down-conversion receivers. Therefore, by employing these schemes, a first of its kind quarter-rate sub-sampling mixer-first direct down-conversion RF front-end is proposed.

Finally, the proposed RF front-ends are implemented in 1.2 V, 65 nm CMOS technology and a test chip is fabricated to verify the performance predicted by analytical equations and circuit-level SpectreRF simulations. Both the proposed sub-sampling RF front-end prototypes are implemented on the same test chip, and the test chip occupies an active area of 0.65 mm^2. The bare dies are directly attached to FR4 PCB and wire bonded to measure the performance of the test chip. The performance of both the RF front-ends is measured individually using various test setups. Verifying the results on four different

chips shows that the first RF front-end offers a wide-band operation from 0.4 - 1 GHz by tuning sampling frequency from 0.32 - 0.8 GHz with a minimum noise figure of 6.5 dB, 15.1 dB conversion gain and 50 dB third harmonic rejection. The proposed RF front-end exhibit IB-IIP_3 of +10 dBm OB-IIP_3 and +20 dBm. The second RF front-end offers wide-band operation over the frequency band 0.4 - 1.8 GHz by tuning a sampling frequency from 0.13 - 0.6 GHz with a bandwidth of 90 MHz. The receiver has a DSB noise figure of 4.7 dB, a conversion gain of 22 dB, an IB-IIP_3 of -1 dBm and OB-IIP_3 of +8 dBm. The switch-capacitor blocks in the first architecture consume 400 μW, and the second architecture consumes a power of 800 μW, which makes both the proposed switch-capacitor-based sub-sampling mixer-first RF front-ends suitable for low-power applications.

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List of Abbreviations

LO	Local oscillator
NF	Noise figure
CG	Conversion gain
P1dB	1dB compression point
IIP3	Input third order intercept point
HTF	Harmonic transfer function
SNR	Signal-to-noise-ratio
SS	Sub-sampling
QRSS	Quarter-rate sub-sampling
LNA	Low noise amplifier
RF	Radio frequency
IF	Intermediate frequency
BB	Base band
HR	Harmonic rejection
HRR	Harmonic rejection ratio
LR-WN	Low rate wireless network
EVM	Error vector magnitude
ADC	Analog to digital converter
DAC	Digital to analog converter
PA	Power amplifier
MOS	Metal oxide semiconductor
CMOS	Complementary metal oxide semiconductor
SDR	Software-defined-radio
S/H	Sample and hold
Q	Quality factor

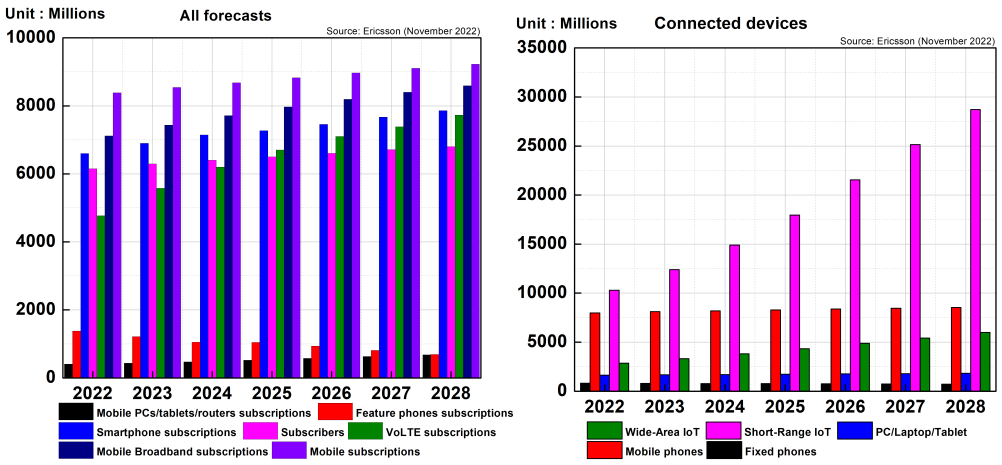
FIR	Finite impulse response
WLAN	Wireless local area network
NPF	N-path filter
TIA	Trans impedance filter
CT	continuous time
DT	Discrete time
SC	Switch-capacitor
I/ Q	In-phase and Quadrature phase
LNTA	low noise trans-conductance amplifier

Chapter 1

Introduction

1.1 Trends in Wireless Communications

Global mobile subscriptions are forecasted to reach 9.2 billion by the year 2028 as shown in Fig. 1.1(a). The fifth-generation technology-based connections are expected to occupy 54 % of the share of mobile traffic and 80 % of fixed wireless access (FWA) connections[1]. The FWA provides a high-speed data transfer to the customers over the air with the help of fixed base stations connected to a network. These base stations offer high-speed wireless connectivity to remote areas without proper infrastructure. In addition, the number of connected IoT devices over mobile networks is around 2.7 billion, and it is projected to reach 5.5 billion in 2028, as shown in Fig. 1.1(b). These statistics reveal the need for flexible radio with a programmable or re-configurable RF front-end to support increased spectrum congestion and multi-band operation to accompany multiple standards using a single receiver. The need for multi-standard operation has led researchers to propose the idea of software-defined radio(SDR).



(a) (b)

Figure 1.1: (a) Global forecast of different device subscriptions (b) connected devices[1]

The concept of SDR is placing the analog-to-digital converter(ADC) just after the antenna receiver[2] and digitizing all the received bands. However, the ADC operating at high frequency imposes impractical power constraints on the ADC[3]. The alternative to an SDR is a flexible radio that supports a multi-band operation with less power dissipation and minimum hardware is the closest possible version of an SDR, which is a digitally intensive receiver. A switch-capacitor based receiver RF front-end provides programmable wide-band operation and consumes very low power makes it digitally intensive RF front-end.

This chapter introduces digitally intensive switch-capacitor RF front-ends in Section 1.2, followed by the classification of the RF front-end architectures based on down-conversion frequency in Section 1.3. Then a brief literature survey on the sub-sampling and RF sampling switch-capacitor RF front-ends is presented in Section 1.4. Afterwards, Section 1.5 presents the research gaps among the reported RF front-ends architectures and thesis objectives are presented. The concept of proposed sub-sampling digitally intensive mixer-first RF front-ends is explained in Section 1.6. Thesis contributions and organization of the thesis are presented in Section 1.7 and Section 1.8, respectively.

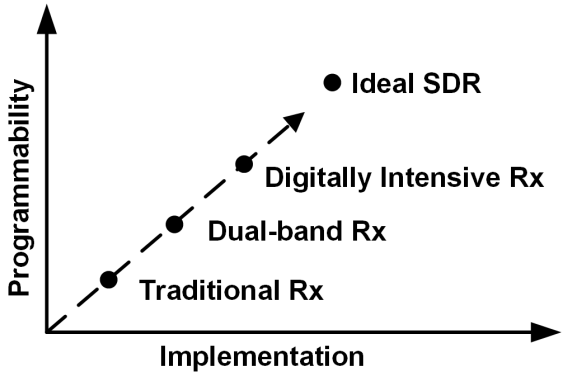


Figure 1.2: Architectural evolution of the receiver RF front-end

1.2 Digitally Intensive Switch-Capacitor RF Front-Ends

The quest for software-defined radio has led researchers to propose various receiver architectures, from traditional single-band radios to digitally intensive architectures, shown in Fig. 1.2. A conceptual representation of an ideal SDR contains an analog-to-digital converter(ADC) and digital-to-analog converter(DAC) just after the antenna before base-band processing as shown in Fig. 1.3(a). To perform the task, it is necessary that the

ADC in the SDR must have extraordinary specifications. In addition, ADC with such high dynamic range and other specifications dissipates hundreds of watts of power for conversion[4]. Therefore, a flexible or re-configurable radio receiver that receives any channel at an arbitrary frequency with less power dissipation and minimum hardware is the closest possible version of an ideal SDR as shown in Fig. 1.3(b).

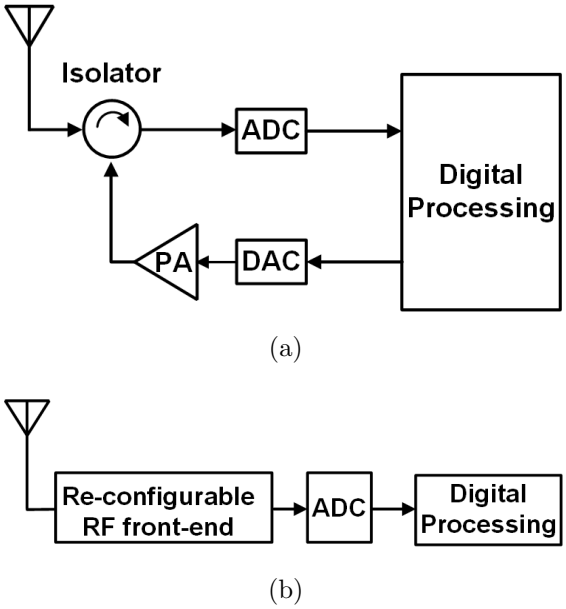


Figure 1.3: Block diagram representation of an (a) ideal [2] (b) and practical software defined radio

The CMOS technology scaling has improved the switching characteristics of a MOS transistor[5]. The rise time and fall time of the transistor switches in the advanced nanometer design are in the order of tens of picoseconds. These rise and fall times offer good timing accuracy to support operation at high frequencies. In addition, modern lithography techniques offer a wide range of capacitor ratios[6]. These advancements have benefited from realizing re-configurable RF front-ends using switch-capacitor mixers and filters. A switch-capacitor mixer-first RF front-end provides performance tunability over a wide frequency range by tuning sampling frequency. This property of switch-capacitor RF front-ends makes them digitally intensive. Therefore, a digitally intensive switch-capacitor radio architecture is the closest equivalent to an ideal software-defined radio(SDR) as shown in Fig. 1.3(b). There are switch-capacitor RF front-ends proposed in the literature which are based on RF sampling down-conversion and sub-sampling. The down-conversion principle of both the RF sampling and sub-sampling based switch-capacitor RF front-ends and the differences among the implementation are explained below.

1.2.1 RF Sampling Based Switch-Capacitor RF Front-Ends

RF sampling-based switch-capacitor front-ends require a sampling frequency greater than or equal to the input RF frequency to implement down-conversion and filtering using N-path mixers and filters, respectively. The N-path implementation of the mixer and filters have advantages in terms of noise figure, tunable high-Q bandwidth, and impedance matching. However, the N-path topology requires precise N-phase non-overlapping clocks for operation, and to generate precise multi-phase non-overlapping clocks, clock dividers are required. To generate non-overlapping clocks with a frequency, f_s, the dividers require a reference clock frequency of at least $Nf_s/2$. Hence, the power consumption of these non-overlapping clock generation and distribution circuitry increases with the increasing f_{RF} since the corresponding sampling frequency also increases. In addition, the stringent jitter requirements increase the power consumption of the frequency synthesizers at high frequencies. Therefore, the power consumption of the clock generation circuit is no longer negligible since it increases with the input RF frequency f_{RF}.

1.2.2 Sub-Sampling Based Switch-Capacitor RF Front-Ends

Sub-sampling down-conversion requires a sampling frequency less than the input RF frequency leading to the reduced power consumption of the frequency synthesizer, non-overlapping clock generation, and distribution circuitry[7, 8]. The theory of band-pass sampling states that *"for uniform sampling states that the signal can be reconstructed if the sampling rate is at least* $f_s = \frac{2f_u}{n}$*, where 'n' is the largest integer within* $\frac{f_u}{BW}$[7]". Where 'f_u' is the maximum frequency and *'BW'* is the bandwidth of the input band-pass signal. This sampling condition is analogous to the low pass sampling, which has a condition for sampling $f_s > 2f_u$, where the input signal's bandwidth is $[0, f_u]$. On the other hand, the quadrature sampling case of band-pass sampling states that if the sampling frequency is selected from Eq. 1.1, the input signal gets down-converted to IF, and the alternative samples at the output are in quadrature.

$$\begin{aligned} f_s &= \frac{4f_{RF}}{2k+1}; k = 0, 1, 2, 3 \ldots \\ f_{IF} &= \min\left(|f_{RF} - nf_s|\right) = f_s/4 \end{aligned} \tag{1.1}$$

Where, f_{IF} represents the intermediate frequency, 'n' represents the harmonic of the

sampling frequency.

The sub-sampling receivers proposed in the literature have emphasized the implementation of down-conversion at both the RF and IF stages down-conversion. These implementations show that sub-sampling down-conversion is a good alternative to RF sampling down-conversion for implementing re-configurable switch-capacitor mixer-first RF front-ends for low-power and wide-frequency band applications. However, the sub-sampling down-conversion is not a popular choice for implementing in mixer-first receivers due to the disadvantage of high noise figure from inherent noise folding and lack of RF port impedance matching because of non-zero IF down-conversion.

1.3 Problem Definition

As explained in Section 1.2.1, RF sampling-based RF front-end requires a sampling frequency greater than the input RF frequency hence it increases the power budget of the receiver. On the other hand, sub-sampling down-conversion has the advantage of operating at a low sampling frequency, thereby reducing the power consumption of clock generation, distribution and frequency synthesizer circuits. However, the sub-sampling down-conversion is not a popular choice for implementing in mixer-first receivers since the sub-sampling down-conversion is inherently heterodyne in nature and high noise figure[9, 10]. As a consequence of non-zero IF down-conversion, the passive mixer transparency property can not be exploited for providing impedance matching at the RF port by impedance translation. Therefore, it is required to address the problems of sub-sampling down-conversion, such as non-zero-IF down-conversion, high noise figure and lack of impedance matching to make it a suitable alternative to RF sampling-based receivers front-ends.

1.4 Literature Survey

In recent years, there has been increasing research interest in re-configurable RF front-ends with frequency translation features. The advancements in CMOS technology scaling improved the switching property of the MOS transistor; hence the switch-capacitor circuits, such as passive mixers and filters, support wide-band operation. In a receiver, employing switch-capacitor circuits at the RF facilitates programmable multi-band operation using a single RF front-end. This section gives an overview of the existing switch-capacitor-

based sub-sampling RF front-end architectures [9–11] along with the RF sampling-based switch-capacitor RF front-end architectures [5], reported in the literature.

1.4.1 Switch-Capacitor Sub-Sampling RF Front-Ends

Sub-sampling down-conversion employs a sampling frequency which is lower than twice the highest frequency of the input RF signal but higher than two times the input RF signal bandwidth. The sub-sampling down-conversion mixer employing a sampling frequency of f_s, translates the input RF signal with a frequency f_{RF} to $\frac{f_s}{4}$, $\frac{3f_s}{4}$, $\frac{5f_s}{4}$,.. etc. In the literature, there are few sub-sampling receivers reported, such as the sub-sampling down-conversion receiver RF front-end architecture [10], which employs two-stage down-conversion to zero frequency down-conversion, the current integrating sub-sampling mixer translates the IF frequency to base-band using a g_m-cell, four-path sub-sampling down-conversion mixer and complex filter[11], and the dual-band down-conversion receiver employed two-stage down-conversion schemes for each band[9].

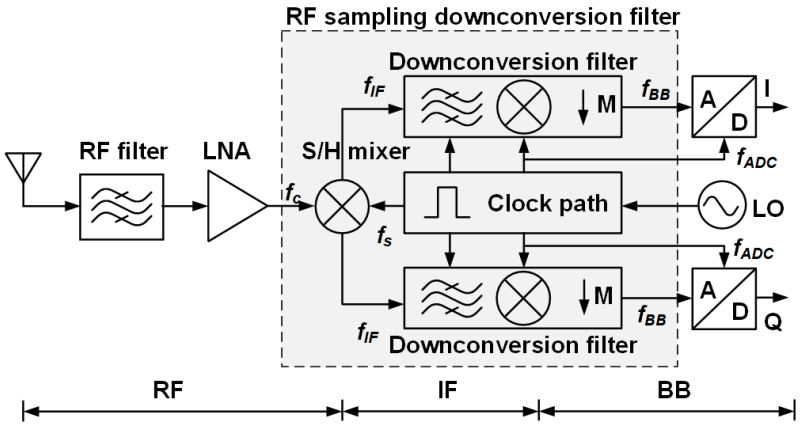


Figure 1.4: Block diagram of the sub-sampling receiver RF front-end[10]

1.4.1.1 Heterodyne Sub-Sampling Receiver in 0.18-μm CMOS

The heterodyne switch-capacitor sub-sampling receiver reported in [10] employed a two-stage discrete-time quadrature down-conversion mixing scheme. The RF front-end contains an RF filter, a tuned LNA, and a switch-capacitor sub-sampling mixer followed by a switch-capacitor decimation filter, shown in Fig. 1.4. The sub-sampling down-conversion receiver architecture is designed for 2.4 GHz IEEE 802.11b/g standard wireless local area network (WLAN) applications in 0.18 μm CMOS. The input RF signal received by the

antenna passes through an RF filter which filters the image of the RF signal, the LNA amplifies the output of the filter, and then it is fed to a single-path sample-hold(S/H) quadrature down-conversion mixer. As proposed in [10], the S/H mixer translates the input RF signal of 2.4 GHz to an intermediate frequency (IF) depending upon the selection of sampling frequency given by Eq. 1.1. For example, the RF signal gets translated to an IF of 268 MHz for a sampling frequency of 1.072 GHz and to an IF of 142 MHz for a sampling frequency of 547.5 MHz. The selection of low sampling frequency, such as 547.5 MHz, translates the input to low IF compared to 1.072 GHz. However, selecting a low sampling frequency of 567.5 MHz translates the copies of RF down-conversions closer compared to the 1.072 GHz, requiring a high-Q RF filter. The output of the mixer is further down-converted to baseband by the switch-capacitor decimation filter. The sampling frequency of the filter is 89.5 MHz, which is obtained by dividing the mixer clock frequency by 24. This way, the decimation filter offered band-pass filtering and down-conversion using decimation. However, the reported sub-sampling receiver does not provide any gain hence it has a high noise figure of 44 dB, an IIP_3 of +5.5 to +13.5, and low bandwidth of 20 MHz only.

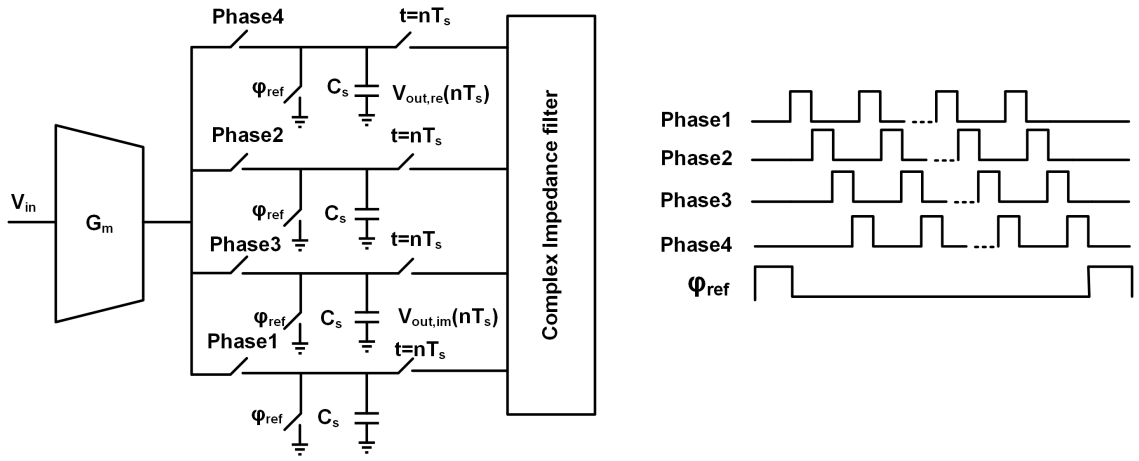


Figure 1.5: Block diagram of the low noise figure sub-sampling mixer[11]

1.4.1.2 A Low Noise Quadrature Sub-Sampling Mixer

A current-mode sub-sampling down-conversion technique is presented in [11]. The current-mode mixer down-converts the input RF/IF signal to IF/BB frequency. The mixer architecture consists of a G_m-cell followed by a four-path switch-capacitor mixer and complex IIR filter as shown in Fig. 1.5. The G_m-cell transforms the input voltage

signal to current, and the switch-capacitor mixer sample the current instead of voltage onto the capacitors. The G_m-cell, along with the current integrating mixer, introduces a low pass sinc-response. The non-overlapping clock scheme of the mixer samples the alternative samples to real and imaginary channels with a time interval of $\frac{T}{4}$. Hence, quadrature down-conversion is achieved in the proposed scheme by introducing a time delay of t_i between the samples, given by Eq. 1.2. To improve the selectivity, the input current is integrated N-times onto the capacitors, which resembles a bandpass FIR filter. In the end, the output of the sub-sampler is further translated to a desired frequency by decimating the signal.

$$t_i = (\frac{n}{2} \pm \frac{T}{4}), \text{where n=0, 1, 2, 3..etc} \tag{1.2}$$

The down-conversion mixer architecture is implemented in 0.8μm BiCMOS technology. The measured noise figure of the sampler is 10 dB at an output frequency of 13.1 KHz. The main drawback of the work is the high noise figure even employing a G_m-cell at the input of the sampler. In addition, the G_m-cell limits the bandwidth of the sampler and the linearity of the mixer.

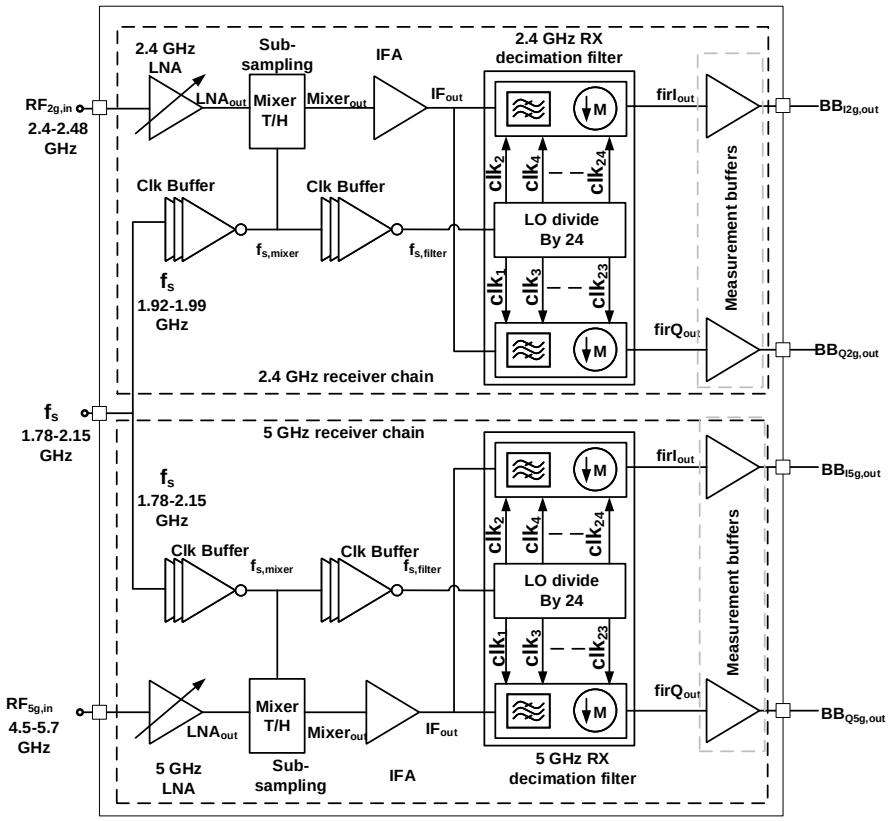


Figure 1.6: Block diagram of the dual-band sub-sampling receiver[9]

1.4.1.3 A Sub-Sampling Dual-Band Tunable Gain Receiver in 65-nm CMOS

A dual-band sub-sampling receiver with a bandwidth of 77 MHz and error vector magnitude(EVM) of -40 dB is proposed for WLAN application in [9]. The dual-band receiver consists of identical sub-blocks and sub-sampling down-conversion employed for down-conversion as shown in Fig. 1.6. The performance of the sub-sampling receiver chain is demonstrated for both the 2.4 GHz and 5 GHz applications. The proposed architecture consists of a tunable LNA, single-path sub-sampling switch-capacitor down-conversion mixer, IF amplifier (IFA) and a switch-capacitor decimation filter. The tunable LNA amplifies the incoming RF signal and provides the required 50 Ω impedance matching, then the single path sub-sampling down-conversion mixer translates the LNA output to an IF frequency of $\frac{f_s}{4}$. The IFA further amplifies the down-converted signal, then the switch-capacitor sub-sampling filter further translates the signal to base-band frequency. The dual-band receiver has a noise figure of 11.5 - 12 dB, a variable gain of 26 - 41 dB and -21 to -8 dBm IIP_3. The main disadvantages of the proposed work are high noise figure and poor IIP_3.

1.4.2 Switch-Capacitor RF Sampling Based RF Front-Ends

In the literature, all the mixer-first receivers employed RF sampling for down-conversion, requiring a sampling frequency greater than or equal to the input RF signal frequency. In contrast to traditional LNA first receivers, switch-capacitor-based receivers such as mixer first receivers and RF front-ends with higher order filtering and mixers [12–14] lack LNA at the RF front-end. These architectures provide higher linearity than LNA first receivers, however lack of RF gain results in a high noise figure. In addition, there are wide-band LNA first receiver architectures reported in the literature, such as [15, 16], which offer wide-band operation, low noise figure and high conversion gain, hence, they are suitable for SDR applications. However, the RF sampling based LNA-first receivers exhibit poor linearity and consume high power at the high frequencies due to low jitter clock requirement for implementing down-conversion[17]. The concept and working principle of various switched-capacitor based mixer-first and LNA-first receivers are presented below.

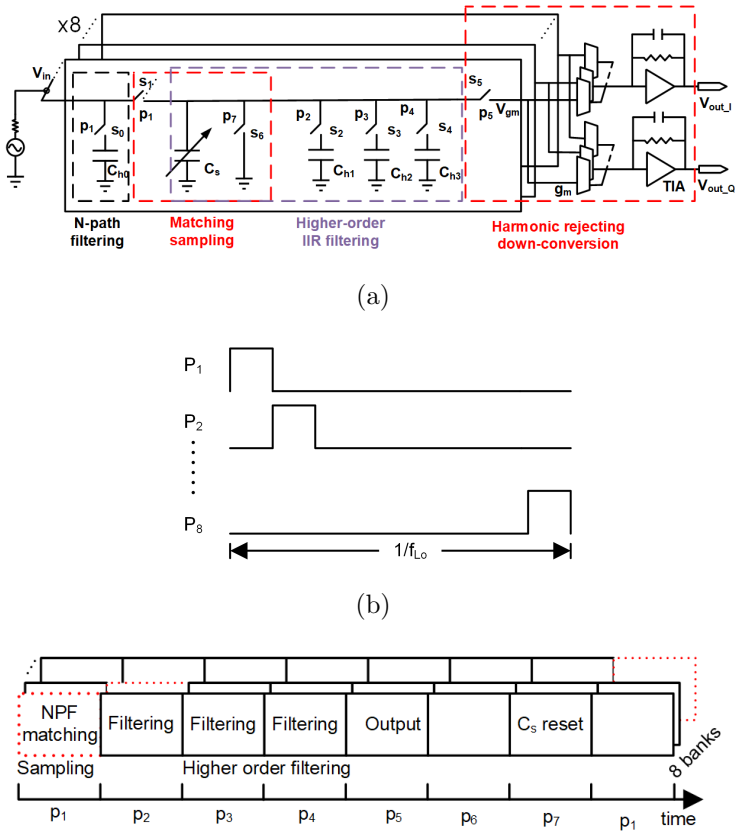


Figure 1.7: (a) Simplified architecture of a single-ended SC RF front-end (b) clock waveform (c) operation of the SC RF front-end[12]

1.4.2.1 A Switched-Capacitor RF Front-End With Embedded Programmable High-Order Filtering

The single-ended version of the switch-capacitor receiver architecture, reported in [12], is shown in Fig. 1.7 (a). The receiver consists of eight single-ended switch-capacitor mixers for sampling and filtering, followed by base-band g_m-cells and trans-impedance amplifiers (TIAs) for harmonic rejection. The switch-capacitor front-end is driven by an eight-phase non-overlapping clock signal p_1 to p_8, shown in Fig. 1.7(b). Each switch conducts for a duration of 12.5 % of $\frac{1}{f_{LO}}$ and the sampling frequency $f_s = 8f_{LO}$. As depicted in Fig. 1.7(c), when p_1 clock is ON, switches S_0 and S_1 conduct and hence the S_0 switches along with C_{h0} realise an RF stage N-path filter(NPF) which attenuates out of band blocker signals. In addition, SC circuit s_0 and C_{hs} provide impedance matching and sample the input RF signal. Hence, s_1 and C_s convert the continuous-time (CT) input RF signal to DT domain. After sampling, the switches s_2 to s_4 and the history

capacitors C_{h1} to C_{h3} and $C_s$well as $C_s(i)$ and $s_6(i)$ realise a high-order discrete-time infinite-impulse-response (IIR) filter. After filtering the switch, s_5 propagates the signal to the g_m cell input nodes. In the end, the g_m cells combine the outputs from all the eight switch-capacitor banks to the in-phase (I) and quadrature (Q) paths and achieve the harmonic-rejecting down-conversion. However, the amount of harmonic rejection depends on the weighing gains of the g_m-cells. The sampling frequency is equal to or greater than the input RF signal, and hence the power consumption of the frequency synthesizer circuit is high.

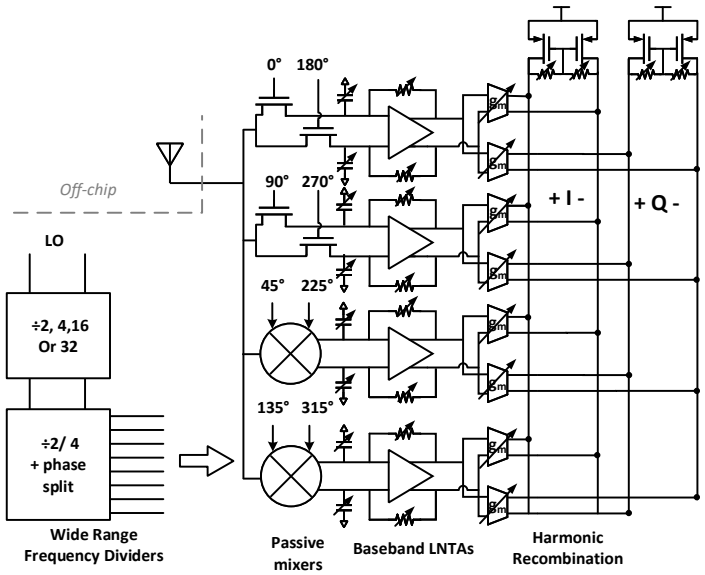


Figure 1.8: Block diagram of the passive mixer-first receiver with widely tunable RF interface[13]

1.4.2.2 A Passive Mixer-First Receiver With Widely Tunable RF Interface

The mixer-first direct down-conversion RF front-end [13] presented several useful concepts of switch-capacitor RF front-end interface, such as tunable input impedance matching by exploiting transparency of passive mixer switches and the input impedance of the baseband amplifier. An eight-path mixer direct down-conversion scheme is employed to translate the input RF to the base-band. These eight-path outputs are amplified by BBLNAs and recombined using g_m-cells to obtain quadrature down-conversion and harmonic rejection, shown in Fig. 1.8. However, it did not discuss the idea of direct down-conversion using harmonics of f_s and its consequences on the noise figure, conversion gain

and RF port impedance matching. In addition, this mixer-first receiver front-ends also employs RF sampling, requiring a sampling frequency greater than the input RF signal frequency, leading to the increased power consumption of clock generation circuits.

1.4.3 Wide-band Receivers for Software-Defined Radio Applications

Typical low noise trans-conductance amplifier(LNTA) first receivers[15, 16] employ a wide-band LNTA followed by a switch-capacitor passive down-conversion mixer as shown in Fig. 1.9. These receiver architectures offer wide-band operation, low noise figure and high conversion gain hence suitable for SDR applications. The working principle and architectural implementation details are explained below.

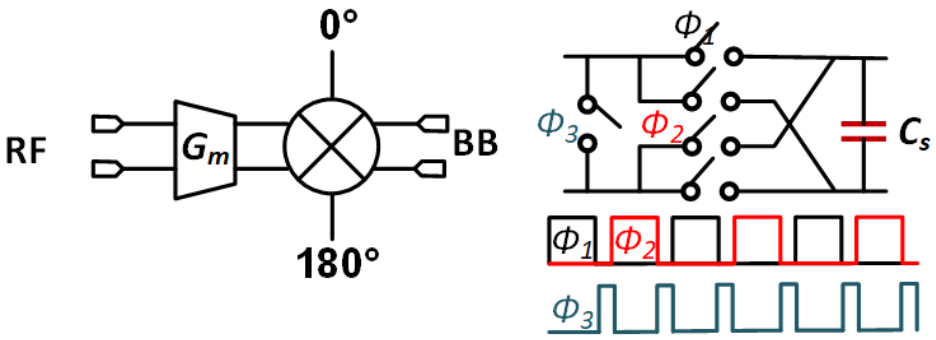


Figure 1.9: Block diagram of LNA first wideband receiver architecture[16]

The trans-conductance (G_m-cell) converts input RF voltage to the corresponding current, and it is fed to a sampling mixer. The down-conversion mixer with a sampling frequency(f_s) translates the amplified input RF signal with frequency, f_{RF} to baseband(BB) at the output. The sampling mixer employs a square wave local oscillator hence mixing a signal by a square wave translates blockers/interferers present at the harmonics of f_s to the baseband, and high conversion gain also amplifies blockers, thereby deteriorating the performance of the receiver. Therefore, to address this issue, multi-path or multi-phase mixing down-conversion mixer topologies are implemented, such as [18], where down-conversion is implemented by three phases 0°, 45°, 90° and weighted by $1 : \sqrt{2} : 1$, and summed to generate a sine wave look like LO signal. The advantage of such LO is harmonic rejection since the Fourier coefficient of the third and fifth harmonics of the resultant LO becomes zero. In a similar approach[19], the down-conversion with a weighing factor of $1 : \sqrt{2} : 1$ is realized in two stages to improve the harmonic rejection. However,

the main disadvantage of such implementation is achieving irrational weighing gains, and two-stage implementations increase the complexity of the receiver.

1.5 Research Gaps and Thesis Objectives

1.5.1 Research Gaps

Based on the literature survey, this section presents the limitations of the sub-sampling receiver implementations [9–11] and RF sampling-based switch-capacitor receiver implementation [12, 13, 16].

As explained in Section 1.4, the sub-sampling down-conversion [10] employs a single-stage switch-capacitor I/Q down-conversion mixer and IF to BB decimation filter for collecting I/Q samples. Furthermore, the low noise quadrature down-conversion mixer [11] employs transconductor 'g_m' for converting the input voltage to the corresponding current, thereby implementing current-mode sampling for down-conversion. The dual-band sub-sampling receiver architecture [9] translates both the 2.4 GHz and 5 GHz bands. These implementations have the same drawback of high noise figure and poor linearity. In addition, the sub-sampling receiver implementations are LNA-first receivers and hence do not provide reconfigurability. Conversely, the mixer-first receivers require a sampling frequency greater than or equal to the input RF frequency and provide reconfigurability over a wide frequency range. The switch-capacitor RF front-ends provide high linearity and a good noise figure of 8 dB or less without a traditional LNA. However, the frequency synthesizers employed in these implementations consume high power since the design is complex and operates at a high frequency. The performance of these RF front-end architectures is compared in Table 1.1.

Therefore, from the literature review presented in Section 1.4, it is evident that there is a need for digitally intensive sub-sampling quadrature down-conversion RF front-end architecture with 50 Ω impedance matching at the RF port. The sub-sampling approach offers a low-power programmable receiver RF front solution for low-power applications since the sampling frequency is less than the input RF, leading to the reduced power consumption of the frequency synthesizer. To address the research gap presented above, the next section presents the proposed digitally intensive sub-sampling receiver architectures.

Table 1.1: Performance summary of the state-of-the-art RF front-ends present in the literature

		[13]	[12]	[20]	[21]	[22]	[23]	[24]	[25]	[10]		[26]*	[9]	
Sampling Scheme		RF sampling							Sub-Sampling					
Architecture		Mixer-first						LNA-first	LNA-first					
Impedance matching w/o LNA		Yes						No	No					
Supply(V)		1.2/2.5	1.2/1.6	1.2	1.2	4.5/2.5	1/1.2	1.5	0.6	1.8		1	1.2	
Technology(nm)		65	40	65	28	130B	28	130	65	180		28	65	
f_{RF}(GHz)		0.1-2.4	0.1-0.7	0.2 - 2	0.2-2	2-11	0.1-2	0.8-4	2.4/2.7	2.4-2.485		58.2-64.8	2.4-2.483	4.5-5.7
f_s(MHz)		0.1-2.4	0.1-0.7	0.2 - 2	0.2-2	2-11	0.1-2	0.8-4	0.3	1072	567	37.2-43.6	1.92-1.99	1.7-2.15
NF(dB)		6-8	9.8-12.7	9.5	7.3-10.6	14±1	7.1-10.3	3.8	6/5	NR		7	11.5	12
BW(MHz)		20	3.2-4.8	25	18	80-260	6.5	6/8	1	NR		NR	20-77	
IIP_3(dBm)		25[a]	24[a]	11	24[a]	20[a]	35[a]	-3.5	NR	+5.5	+13.5	NR	-23 to -8	-21.5 to 8
Gain(dB)		40-70	40	19	40	10-24	16	28	40	-1	1	36	26-40	
Power(mW)	LO	7.2-39.6	7-53	67	3-36	1466-1494	34-96	33[b]	NR	47	43	204[c]	NR	NR
	IF/BB	30	52		100.43	656 674	30	NR	1.3	NA	NA	NA	27.8	27.8
Area(mm^2)		0.75	2.03	0.13	0.48	3.4-5	0.49	0.25	0.35	0.36		NA	0.36	0.36

a: OOB-IIP_3; b: Mixer and non-overlapping clock generation power consumption;

c: Estimated; f: Power consumption including both 4-phase and 8-phase clocks; *: Simulations; NF: Noise figure(SSB); BW: Bandwidth

1.5.2 Thesis Objectives

The main objective of the thesis is to implement a low noise figure, highly linear, impedance matched programmable wide-band sub-sampling mixer-first RF front-end using process scalable circuit components such as switches, capacitors, and CMOS inverters.

The design goals for the proposed sub-sampling RF front-end are considered in terms of sampling frequency used for down-conversion, noise figure, conversion gain, P1dB, IIP_3, impedance matching, and harmonic rejection are provided as follows:

- RF front-end should support programmable or re-configurable wide-band operation.
- Sampling frequency should be less than input RF frequency($f_s < f_{RF}$).
- Noise figure should be less than the previously reported sub-sampling receivers, i.e., $\leq$ 10 dB.
- IIP_3 should be greater than +0 dBm.
- 50 Ω impedance matching at the RF port.
- Input return loss (S_{11}) should be greater than 10 dB through the band.

1.6 Proposed Solutions

All the mixer-first RF front-ends reported in the literature have employed RF sampling for down-conversion[5]; hence they operate at a sampling frequency equal to or greater than the input RF frequency(f_{RF}), requiring high-performance frequency synthesizers with stringent phase noise, jitter requirements leading to increased power consumption[17]. On the other hand, the sub-sampling class of receivers operate at a sampling frequency less than the incoming f_{RF}, leading to the reduced power consumption of the frequency synthesizer. Additionally, sub-sampling receivers do not suffer from the disadvantages such as DC offset, second-order non-linearity and $1/f$ noise due to non-zero IF. The sub-sampling architectures reported are low-power receivers and multi-standard RF receivers with two mixer stages [9–11, 26, 27]. However, there is no sub-sampling mixer-first receiver architecture reported till date due to the inherent disadvantages such as noise folding leading to high noise figure and lack of impedance matching at the RF port due to non-zero IF. Therefore, by addressing these issues, two re-configurable sub-sampling mixer-first RF front-ends are proposed[28, 29]. This thesis provides a detailed performance analysis of the proposed RF front-ends in terms of conversion gain, noise

figure, linearity, harmonic rejection and impedance matching.

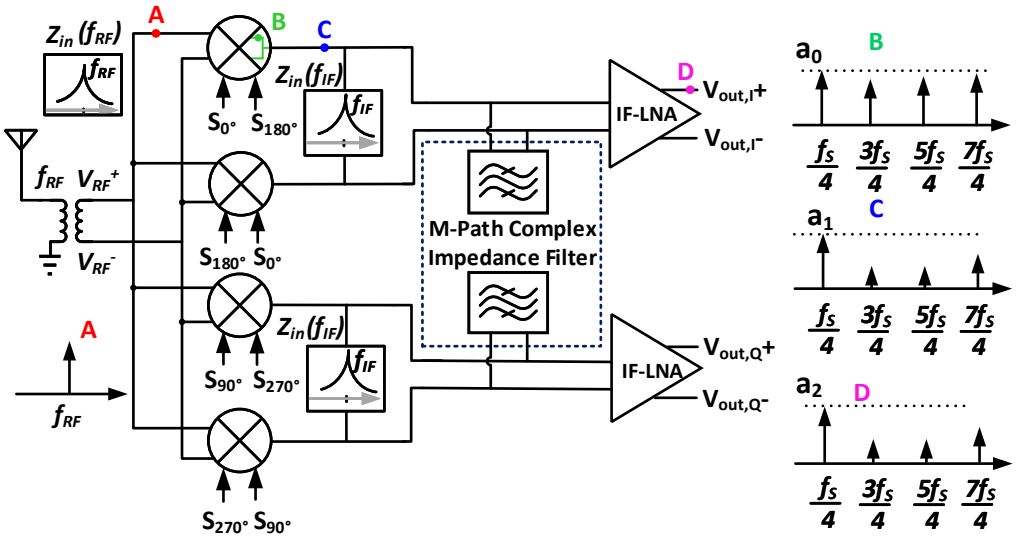


Figure 1.10: Block diagram of the proposed process scalable sub-sampling mixer-first RF front-end

1.6.1 A Process Scalable Architecture for Low Noise Figure Sub-Sampling Mixer-First RF Front-End

The block diagram of the proposed sub-sampling mixer-first RF front-end architecture is shown in Fig. 1.10. The proposed RF front-end addresses two important issues in sub-sampling mixers for making them ready to be deployed as mixer-first sub-sampling RF receivers. Firstly, a multi-path down-conversion mixer scheme is proposed to reject the selected IF odd-harmonics of $f_s/4$, thereby alleviating the effect of noise folding, leading to a low noise figure mixer. Secondly, the impedance matching problem of sub-sampling down conversion is addressed by having an IF stage impedance centred at frequency $f_s/4$ using an M-phase switch-capacitor band-pass filter and an IF-LNA. A complete analysis using analytical equations of the performance metrics such as noise figure, input impedance, frequency plan and its effect on noise figure, the magnitude of harmonic rejection, conversion gain and linearity are presented. To validate the performance predicted by analytical equations as well as to explain the architecture, strategies and principles, a sub-sampling mixer-first RF front-end architecture is implemented in 1.2 V, 65 nm CMOS. The proposed RF front-end employs process scalable circuit components like switches, capacitors

and inverters, and hence RF front-end scales very well with the technology. It is established that the performance predicted by analytical equations and SpectreRF simulations at the architecture level and at the circuit level is in close agreement with test chip measurement results.

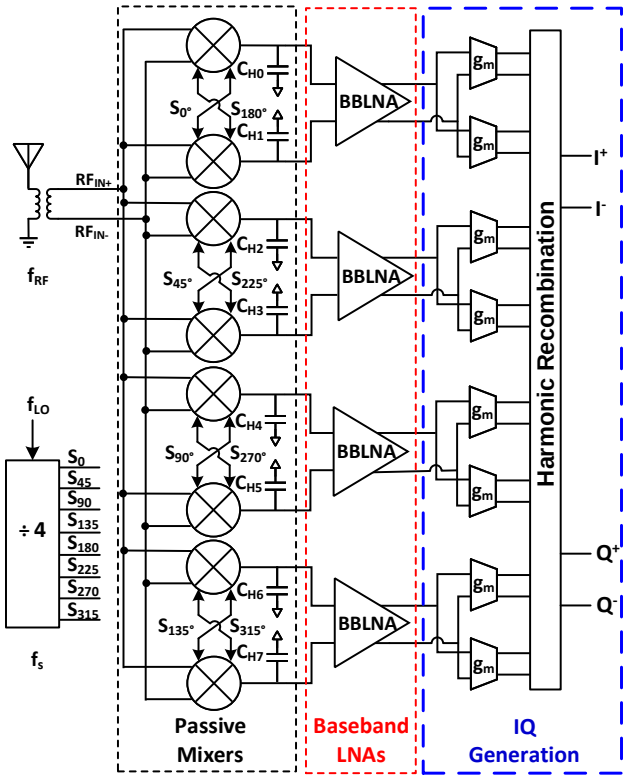


Figure 1.11: Block diagram of the proposed sub-sampling direct down-conversion mixer-first receiver architecture

1.6.2 Digitally Intensive Sub-Sampling Mixer-First Direct Down-Conversion RF Front-End

The second architecture proposed in this work addresses the non zero-IF down-conversion problem of sub-sampling by employing direct down-conversion using harmonics of sampling frequency f_s. The block diagram of the proposed digitally intensive sub-sampling mixer-first direct down-conversion RF front-end is shown in Fig. 1.11. The main contribution of the second architecture includes a sub-sampling direct down-conversion scheme and 50 Ω impedance matching at the RF port by using sub-sampling frequency f_s equal to one-third of f_{RF} and an eight-path mixer. In the proposed scheme, the third har-

monic of the f_s is used for direct down-conversion to zero-IF and down-conversions from the fundamental and fifth harmonic of f_s are marginally attenuated. This work proposes a first-of-its-kind sub-sampling direct down-conversion mixer-first RF receiver front-end. The architecture is simulated, and the performance is verified using technology scalable components like switches, capacitors, and inverters. It is observed that the proposed digitally intensive architecture performance predicted by analytical equations and Spectre simulations is in agreement with the test chip measurement results.

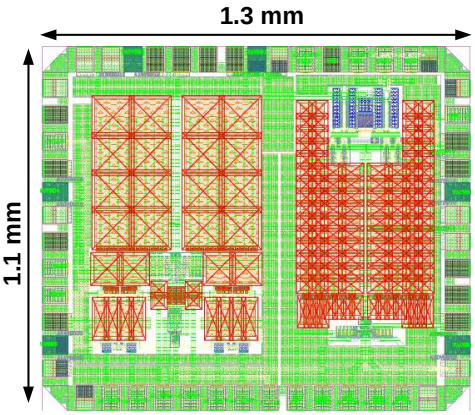
1.7 Thesis Contribution

This thesis proposes two digitally intensive process scalable sub-sampling reconfigurable mixer-first RF front-ends. These RF front-ends are designed using process scalable circuit components like switches, capacitors and inverters, and hence the proposed architecture scales very well with the technology.

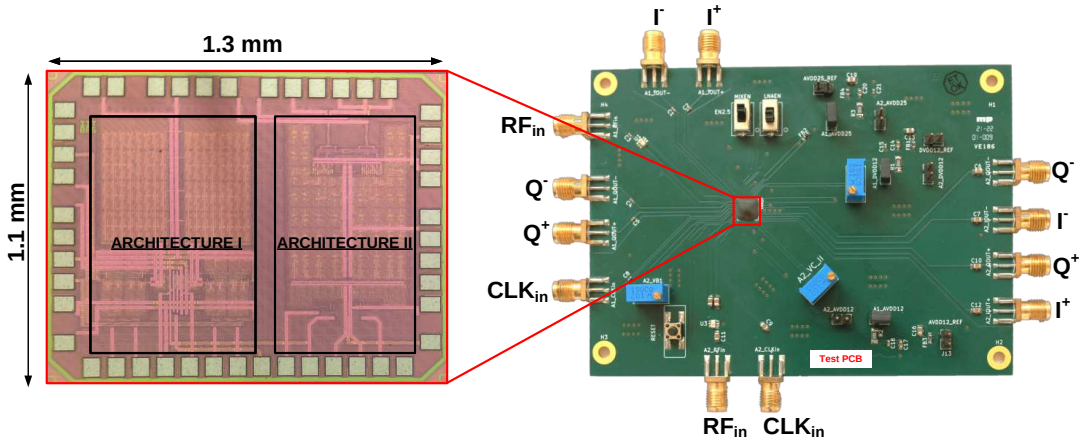
The main contributions of the thesis are listed below.

1. As explained in Section 1.6.1, the process scalable low noise figure sub-sampling mixer-first RF front-end addresses the issues of noise folding and impedance matching. A scheme to reject the selected IF odd-harmonics of $f_s/4$ by multi-path sampling is proposed, alleviating the effect of noise folding, thereby leading to low noise figure sub-sampling mixer-first RF front-end. The impedance matching issue of sub-sampling down-conversion is addressed by proposing an IF-stage impedance by using a combination of the M-phase band-pass filter and the IF-LNA.
2. As explained in Section 1.6.2, the digitally intensive sub-sampling mixer-first direct down-conversion RF front-end architecture proposes a scheme for direct down-conversion sub-sampling RF front-end and also another scheme for impedance matching at the RF port by using sub-sampling frequency(f_s) harmonics and an eight-path mixer. In both these schemes, the third harmonic of the f_s is used for direct down-conversion to zero-IF. Hence, the proposed sub-sampling receiver architecture outperforms RF sampling receivers in terms of clock generation circuit power consumption, thanks to the low operating clock frequency of the sub-sampling RF radio.
3. A proof-of-concept test chip containing both the proposed digitally intensive sub-sampling mixer-first RF front-ends has been designed and fabricated in 1.2 V 65

nm CMOS technology. Both the proposed sub-sampling RF front-end prototypes are implemented on the same test chip, and the test chip occupies an active area of 0.65 mm^2. The full-chip layout is shown in Fig. 1.12(a). The bare dies are directly attached to FR4 PCB and wire bonded to measure the performance of the test chip as shown in Fig. 1.12(b).



(a)



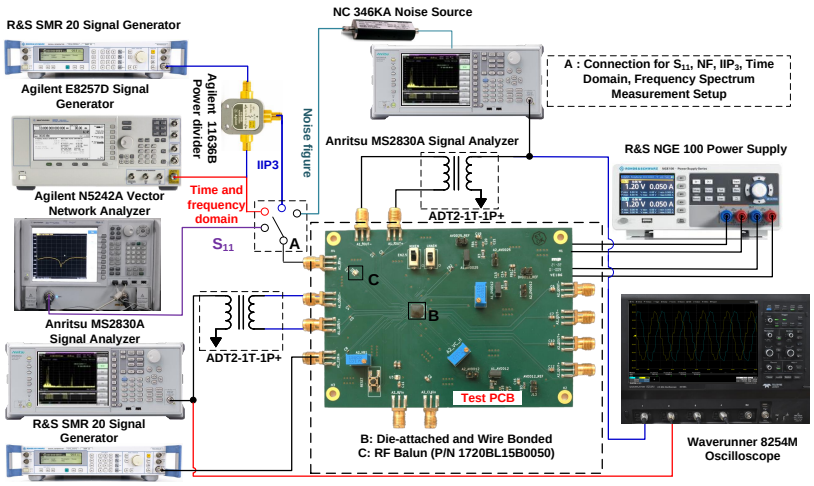
ARCHITECTURE I: A process Scalable Architecture For Low Noise Figure Sub-Sampling Mixer-First RF Front-End
ARCHITECTURE II: Digitally Intensive Sub-sampling Mixer-first Direct Down-conversion RF Front-End

(b)

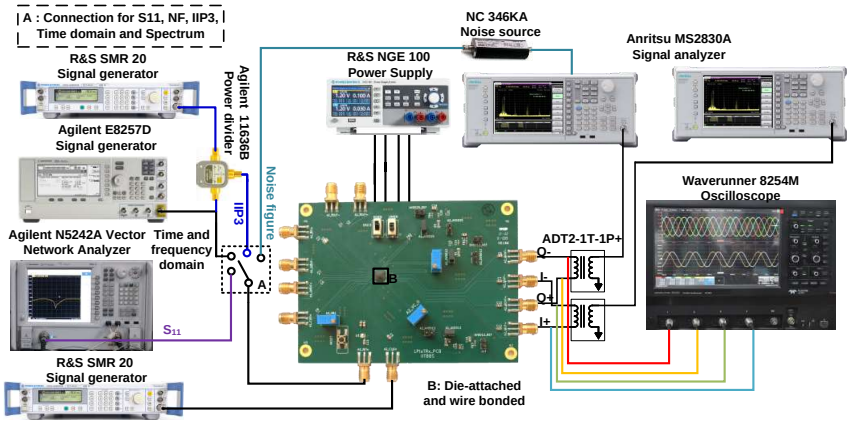
Figure 1.12: (a) Full-chip layout, (b) microphotograph of the bare die and photograph of the test PCB

4. The performance of the proposed sub-sampling mixer-first RF front-ends is measured individually using various test setups, shown in Fig. 1.13(a) and (b). The measured performance of the proposed RF front-ends is in close agreement with the

performance predicted by analytical equations and SpectreRF simulations.



(a)



(b)

Figure 1.13: Test chip measurement setup (a) architecture-I, (b) architecture-II

5. The proposed digitally intensive sub-sampling receiver test chip is designed, simulated, and fabricated chip performance is measured in the lab.

1.8 Thesis Organization

This thesis presents the design and implementation details of the proposed reconfigurable sub-sampling mixer-first RF front-ends.

Chapter 1: Introduction

This chapter provides an introduction to the need for digitally intensive RF front-

ends and the motivation behind undertaking the sub-sampling down-conversion scheme to implement re-configurable RF front-ends, along with the literature survey, objectives and contributions of the thesis.

Chapter 2: A Process Scalable Architecture for Low Noise Figure Sub-Sampling Mixer-First RF Front-End

In this chapter, the concept of the proposed " process scalable architecture for low noise figure sub-sampling mixer-first RF front-end" is presented. This chapter mainly focuses on the implementation details of the multi-path sub-sampling harmonic rejection mixer scheme and the IF stage impedance matching scheme. In addition, the performance of the proposed RF front-end is analyzed using results analytical equations, and 1.2 V, 65 nm CMOS circuit-level performance is also verified using spectreRF simulation. Finally, the overall error vector magnitude (EVM) analysis of the proposed RF front-end is also presented at the end of the chapter.

Chapter 3: Digitally Intensive Sub-sampling Mixer-First Direct Down-Conversion RF Front-End

This chapter presents the concept of the proposed "digitally intensive sub-sampling mixer-first direct down-conversion RF front-end". In this chapter, the implementation details of the proposed eight-path mixer-based approach to achieve direct down-conversion and impedance matching using the third harmonic of f_s are presented. In addition, the performance of the proposed RF front-end is analyzed using results analytical equations, and 1.2 V, 65 nm CMOS circuit-level performance is also verified using spectreRF simulation. Finally, the overall error vector magnitude (EVM) analysis of the proposed RF front-end is also presented at the end of the chapter.

Chapter 4: CMOS Implementation of Sub-Sampling RF Front-end Architectures

The circuit and layout implementation details of the two sub-sampling RF front-ends proposed and presented in Chapter 2 and Chapter 3 of the thesis are presented in this chapter. In addition, the post-layout performance results and summary of both the proposed RF front-ends are also provided. Finally, the full-chip layout implementation details, individual sub-block placement and details of the input and output pins of both the RF front-ends are also provided in Chapter 4.

Chapter 5: Measurement Results and Discussion

The test chip containing both the proposed sub-sampling mixer-first RF front-ends is fabricated in 1P9M TSMC 65-nm CMOS technology. This chapter presents the fabricated test chip measurement results for both the RF front-ends based on [30] and [31] and the discussion of the measurement results. Initially, the details of the PCB designed to test the fabricated chip performance and the details of measurement setups are presented. Next, the measured performance of the proposed process scalable architecture for low noise figure sub-sampling mixer-first RF front-end in terms of IF output frequency spectrum, harmonic rejection, conversion gain, noise figure, S_{11}, P1 dB and IIP_3 is presented. Similarly, the measurement setup used for testing the performance of the proposed digitally intensive sub-sampling mixer-first direct down-conversion RF front-end is also provided. In addition, the measured performance of the proposed direct-down conversion receiver, in terms of baseband output frequency spectrum, conversion gain, noise figure, S_{11}, P1dB and IIP_3 is presented in the second half of Chapter 5. Finally, the performance comparison of both the proposed RF front-ends with the state-of-the-art RF front-ends is presented at the end of the chapter.

Chapter 6: Summary, Conclusions and Future Work

This chapter summarises the outcomes based on the work reported in chapters 2 to 5 of the thesis and discusses the future possible work, which includes further optimization of IF-LNA performance to reduce the power consumption, designing of divider-less non-overlapping clock generation circuit and achieving impedance matching at the higher harmonics of f_s, i.e., beyond the third harmonic of f_s.

Chapter 2

A Process Scalable Architecture for Low Noise Figure Sub-Sampling Mixer-First RF Front-End

This chapter presents the concept of the process scalable architecture for low noise figure sub-sampling mixer-first RF front-end. Section 2.1 explains the idea of sub-sampling wireless links for low-power radios, which includes the low-power paradigm of sub-sampling down-conversion and the proposed RF front-end scheme. In addition, as explained in Section 1.5.2, the performance analysis of sub-sampling mixer-first RF front-end in terms of proposed harmonic rejection scheme, noise figure, conversion gain and linearity are presented in Section 2.2. The proposed impedance matching scheme for sub-sampling mixer-first RF front-end is provided in section 2.3. The system-level EVM performance of the proposed RF front-end using block-level parameters is presented in Section 2.4 and Section 2.5 concludes the chapter.

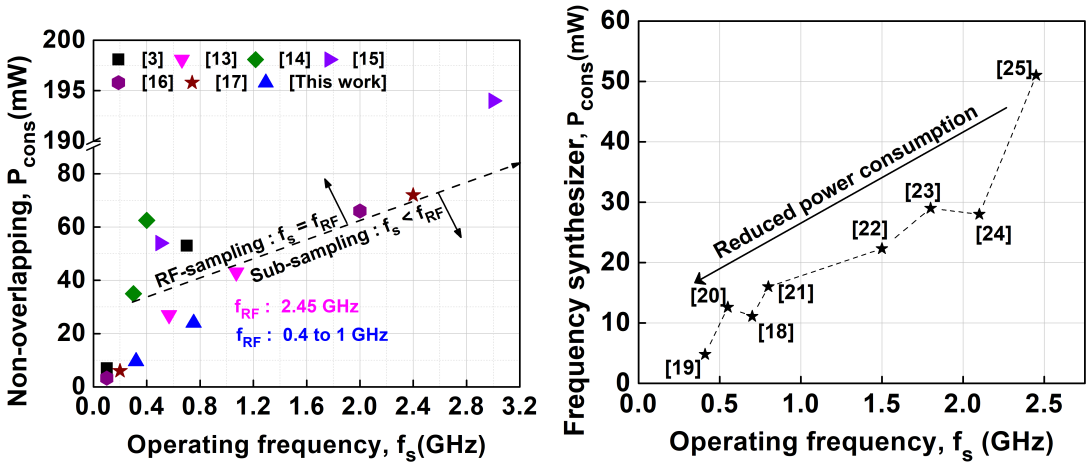
2.1 Sub-Sampling Wireless Links for Low-Power Radios

This section presents the sub-sampling down-conversion paradigm for low-power applications and the noise figure requirements for the low-rate wireless network(LR-WN) specifications.

2.1.1 Sub-Sampling Down-Conversion: A Low-Power Paradigm

The LR-WN technology demands low-power operation with low-data rates. The traditional receiver architectures do not support this low-power paradigm of LR-WN technology. This section looks into the power budgeting of different blocks in a receiver. The total power consumption in a receiver includes the power consumption of the major subsystems, such as a receiver, sampling clock generation, and distribution. Specifically for sampling-based RF radios, LO generation involves non-overlapping, multi-phase clock generation,

distribution, and realization of a frequency synthesizer.



(a) (b)

Figure 2.1: Power consumption of the (a) non-overlapping multi-phase clock generation, distribution circuits, (b) sampling frequency synthesizers versus their operating frequency.

The power consumption of the non-overlapping, multi-phase clock generation, distribution for different operating frequencies of a mixer-first RF sampling receiver architectures[10, 12, 32–35] is shown in Fig. 2.1(a). It is observed that at higher operating frequencies, the power consumption of the non-overlapping, multi-phase clock generation, distribution is almost equal to the power consumption of the receiver circuit. For example, in[12], the clocking circuits operating in the frequency range of 0.1 GHz to 0.7 GHz consume power in the range of 7 mW to 53 mW. At this rate, the power consumption of non-overlapping, multi-phase clock generation and distribution circuit exceeds the receiver power consumption.

On the other hand, published frequency synthesizers[36–43] power consumption versus their operating frequency is shown in Fig. 2.1(b). This graph reveals that the power consumption of the frequency synthesizer decreases with the decreased operating frequency. Therefore, sub-sampling receivers are a good choice for LR-WN technology applications, since the power consumption of non-overlapping, multi-phase clock generation, distribution circuits and realization of a frequency synthesizer, dramatically drops at low sampling frequencies. This analysis demonstrates that one of the elegant ways of reducing the total power consumption of the receiver is by deploying a low sampling frequency RF radios enabled by sub-sampling.

Sub-sampling down-conversion receivers[9, 10, 29] employ a low-frequency clock which depends on the signal bandwidth rather than the highest frequency component at the RF receivers. Hence, it has an inherent advantage in terms of a less complex, less power-hungry sampling frequency generator operating at a low sampling frequency. For example, the power consumption of sub-sampling implementation [10] has a reduced power consumption since the $f_s < f_{RF}$ compared to the RF sampling-based implementations. Thus, it is evident that the sub-sampling down-conversion architectures are power efficient, and hence they are suitable for deploying in the LR-WN networks leading to longer battery life. However, the direct consequence of the sub-sampling is inherent noise folding and hence high noise figure[9, 10]. This issue is addressed in this work by using a multi-path harmonic rejection scheme along with an impedance matching scheme.

2.1.2 Sub-Sampling RF Front-End for Low-Power Application

The proposed sub-sampling RF front-end has two major contributions, one, a low noise figure harmonic rejection mixer scheme to alleviate the problem of noise folding, and two, an IF stage impedance matching scheme for the sub-sampling non-zero IF receivers. These two schemes make the sub-sampling down-conversion suitable to deploy in mixer-first receivers. The proposed sub-sampling mixer-first RF front-end consists of a four-path sub-sampling mixer IF stage switch-capacitor filters and IF-LNAs as shown in Fig. 1.10. The four-path mixer down-converts the incoming RF signal to IF and offers harmonic rejection leading to a low noise figure. The IF-LNA, in combination with the switch-capacitor filter, offers the required gain at IF and impedance matching at the RF port. The impedance realized by this combination at IF is frequency translated to f_{RF} by the transparency property of the passive mixer.

The proposed architecture is realized for the LR-WN standard in the frequency band from 0.4-1 GHz with a target sensitivity of -92 dBm. Specifically, the architecture is realized for 860 MHz and 940 MHz bands for a target bandwidth in the range from 20-50 MHz. Different system-level physical layer parameters specified by the IEEE 802.15.4 standard are given in Table. 2.1. The required noise figure is calculated by Eq. (2.1)[44], where P_{min} is the minimum power level at the input of the receiver, BW is the transmission bandwidth, and SNR_{min} is the minimum signal-to-noise ratio.

$$NF(dB) = P_{min}(dB) + 174(dBm/Hz) - 10log_{10}(BW) - SNR_{min}(dB) \tag{2.1}$$

Table 2.1: Parameters of IEEE 802.15.4 Standard

Parameter	Specification
Frequency range (GHz)*	0.16 - 2.4
Typ. bandwidth (MHz)	50
Sensitivity(dBm)	-92
Noise figure(dB)**	<12
$\mathrm{IIP}_3(dBm)$	>-10

* Various frequency bands

** Estimated

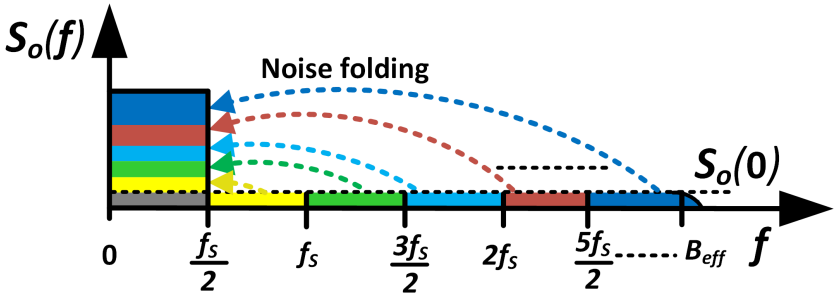


Figure 2.2: Noise folding in the sub-sampling down conversion.

The noise figure for a minimum SNR of -5 dB [45], and for a typical bandwidth of 50 MHz is 10 dB. Therefore, the target noise figure for the proposed RF front-end is $<$ 10 dB to achieve the needed sensitivity of -92 dBm.

2.2 Harmonic Rejection and Noise Figure of Sub-Sampling Mixer-First RF Front-End

2.2.1 Single Path Sub-Sampling Mixer

Generally, a switch-capacitor single-path mixer is sufficient to implement the sub-sampling down-conversion [9, 10]. In sub-sampling, the down-conversion mixer translates the input RF signal to IF at the odd harmonics of $f_s/4$. For an input RF signal with frequency f_{RF}, the mixer effective tracking bandwidth B_{eff} is usually twice the f_{RF}. Hence, the input noise within B_{eff} folds back into the first Nyquist zone during the

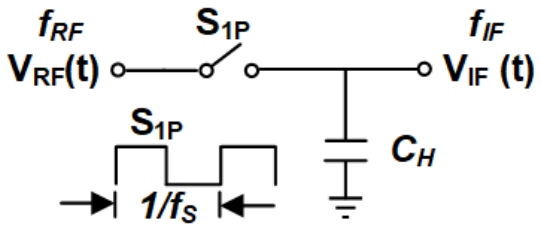


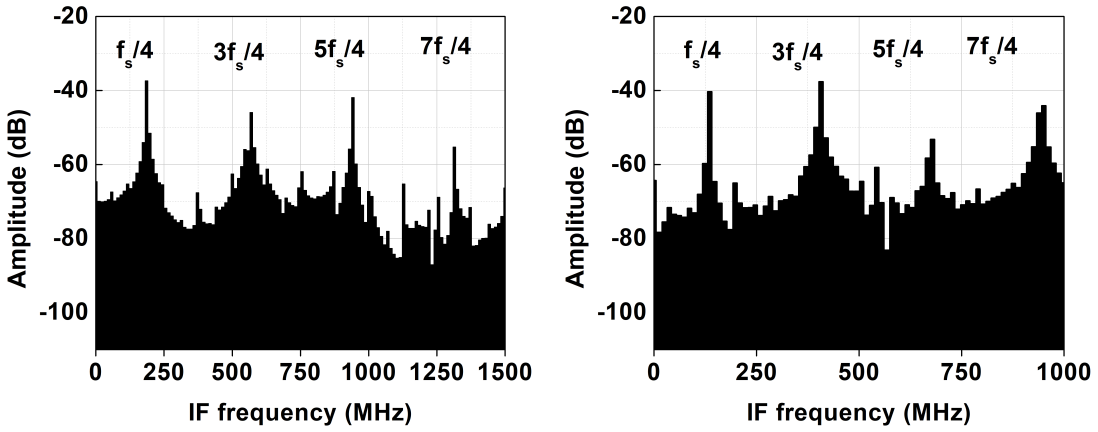
Figure 2.3: Single path sub-sampling mixer.

down-conversion, as shown in Fig. 2.2. Thus, single-path sub-sampling mixers suffer from inherent noise folding, leading to a high noise figure. On the contrary, the RF sampling-based mixer translates the IF output to multiples of sampling frequency F_s, which is comparable to B_{eff}, thereby reducing the effect of noise folding at the desired IF output. The amount of noise aliasing or the number of times noise folds back into the first Nyquist zone depends on the ratio of F_s to f_s, where F_s is the RF sampling frequency, and f_s is the sub-sampling frequency.

The single-path switch-capacitor sub-sampling down-conversion mixer is shown in Fig. 2.3. In sub-sampling, for a given f_{RF}, the sampling frequency is selected from Eq. (2.2)[10], and the mixer output is generated at the odd integer multiples of $f_s/4$, such as $3f_s/4$, $5f_s/4$, and $7f_s/4$. These harmonics at the IF are the frequency translations due to the harmonics of sampling frequency(f_s). Hence, IF harmonics other than the $f_s/4$, located nearer to the $f_s/4$ must be sufficiently suppressed prior to further processing, such as amplification, filtering and decimation.

$$\begin{aligned} f_s &= \frac{4f_{RF}}{2k+1}; k = 1, 2, 3... \\ f_{IF} &= min(|f_{RF} - nf_s|); n = 0, 1, 2, 3... \\ &= f_s/4 \end{aligned} \tag{2.2}$$

The frequency response of the single path switch-capacitor mixer has a low pass sinc response; hence, the mixer band limits the thermal noise before the signal sampling. However, the images of the input thermal noise present within the B_{eff} fold into the first Nyquist-band while sampling, as shown in Fig. 2.2. It means that wider B_{eff} captures the noise in the higher Nyquist zones and folds into the first Nyquist band. Thus, the unwanted harmonics and the sub-sampling noise folding degrade the SNR at the mixer output and the degradation of SNR_{out} is given by Eq. (2.3)[46]. Therefore, for a selected



(a) (b)

Figure 2.4: Single path sub-sampling mixer IF output spectrum (a) for an f_{RF} = 940 MHz and f_s of 752 MHz (k = 2), and (b) for an f_{RF} = 940 MHz and f_s of 537 MHz (k = 3).

f_{RF}, as the f_s decreases, the folding factor increases; this results in high noise folding into the first Nyquist band and degrades the SNR_{out}.

$$SNR_{out} = \frac{P_{signal}}{N_{in} + (m-1)N_{out}}; m = floor(\frac{B_{eff}}{f_s}) \tag{2.3}$$

where, P_{signal} is the band-pass signal power, N_{in} is the in-band noise power, N_{out} is the out-of-band noise power, floor(X) rounds the elements of X to the nearest integers towards zero and m represents noise folding factor.

A sub-sampling switch-capacitor single path mixer is implemented in 1.2 V, 65 nm CMOS, and Spectre RF simulations are performed. The IF output simulated spectrums for an f_{RF} of 940 MHz and sampling frequencies of 752 MHz, 537 MHz are given in Fig. 2.4(a), Fig. 2.4(b) respectively. The noise figure of the sub-sampling mixer is calculated from Eq. (2.4)[47] for an f_{RF} of 940 MHz and sampling frequency of 752 MHz is 7.5 dB. Also, from the spectreRF PSS, PNOISE simulations, the noise figure is equal to 7.5 dB. These results show that the switch-capacitor single path sub-sampling mixer noise figure is high due to the inherent noise folding.

$$F_w(f_{IF}) = \left(1 + \frac{R_{on}}{R_s}\right) \cdot \frac{\sum_{n=-\infty}^{+\infty} |H_n(f_{IF})|^2}{|H_w(f_{IF})|^2} \tag{2.4}$$

where, R_{on} is the on-resistance of the MOS transistor of the mixer, R_s is the source

resistance, $H_n(f_{IF})$ is the harmonic transfer function (HTF) of the n^{th} harmonic. $H_w(f_{IF})$ is the HTF of the desired frequency conversion, and w = -1 for f_{RF} of 940 MHz and f_s of 752 MHz.

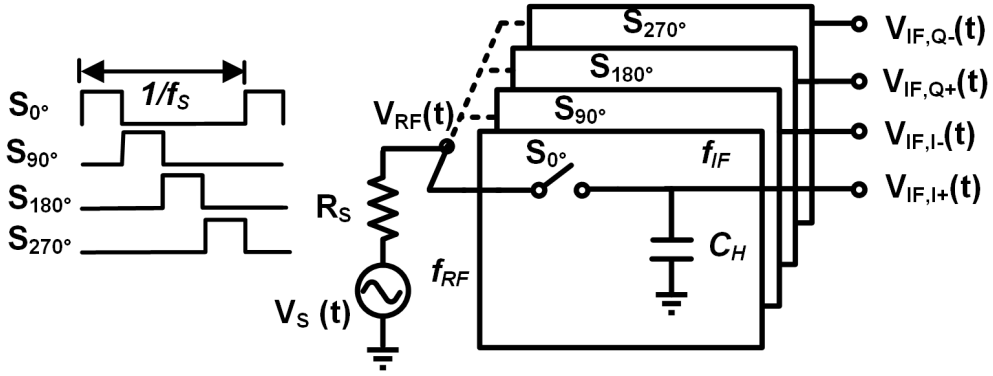


Figure 2.5: Four-path harmonic rejection sub-sampling mixer.

2.2.2 Harmonic Rejection Multi-Path Sub-Sampling Mixer

A multi-path mixer is a parallel combination of the single-path switch-capacitor mixers excited by non-overlapping sampling clocks. It means that an N-path mixer has an N single-path switch-capacitor mixers, and each mixer switch is excited by N non-overlapping clock phases with a duty cycle of $(100/N)\%$. In this work, a four-path mixer is employed, each path has a duty cycle of 25%, and the non-overlapping clocking scheme is shown in Fig. 2.5. In multi-path down-conversion, these non-overlapping clock phases introduce an additional sign change in the Fourier coefficients of the clock, thereby exhibiting a corresponding change in the amplitude of the harmonics at the mixer output. Therefore, these outputs are subtracted to obtain the required harmonic rejection and quadrature down-conversion in the manner explained below.

A single path sub-sampling down-conversion mixer output and the voltage at the sampling capacitor C_H is denoted as $V_{IF}(t)$, given by Eq. (2.5).

$$V_{IF}(t) = a_0 V_{RF}(t) + \sum_{n=1}^{\infty} \left(\frac{a_n A_{RF}}{2} cos(\omega_{RF} - n\omega_s) - \frac{b_n A_{RF}}{2} sin(\omega_{RF} - n\omega_s)t\right) \quad (2.5)$$

where, A_{RF} is the amplitude of the input RF signal, a_n and b_n are the Fourier co-effeicents of the mixer sampling clock.

Similarly, the four-path sub-sampling down conversion mixer has four outputs, and they are denoted by $V_{IF,I+}(t)$, $V_{IF,Q+}(t)$, $V_{IF,I-}(t)$ and $V_{IF,Q-}(t)$, shown in Fig. 2.5.

The in-phase and quadrature-phase IF outputs are obtained by performing the operations ($V_{IF,I+}(t)$ - $V_{IF,I-}(t)$) and ($V_{IF,Q+}(t)$ - $V_{IF,Q-}(t)$) respectively.

These in-phase and quadrature outputs of the multi-path mixer after the harmonic rejection is given by Eq. (2.6).

$$\begin{aligned} V_{IFI/Q}(t) = \frac{A_S A_{RF}}{\pi}\big[\pm cos(\omega_{RF} - \omega_s)t - sin(\omega_{RF} - \omega_s)t \\ \mp \frac{1}{3}cos(\omega_{RF} - 3\omega_s)t - \frac{1}{3}sin(\omega_{RF} - 3\omega_s)t + ..\big] \end{aligned} \tag{2.6}$$

where A_S is the amplitude of the mixer sampling clock.

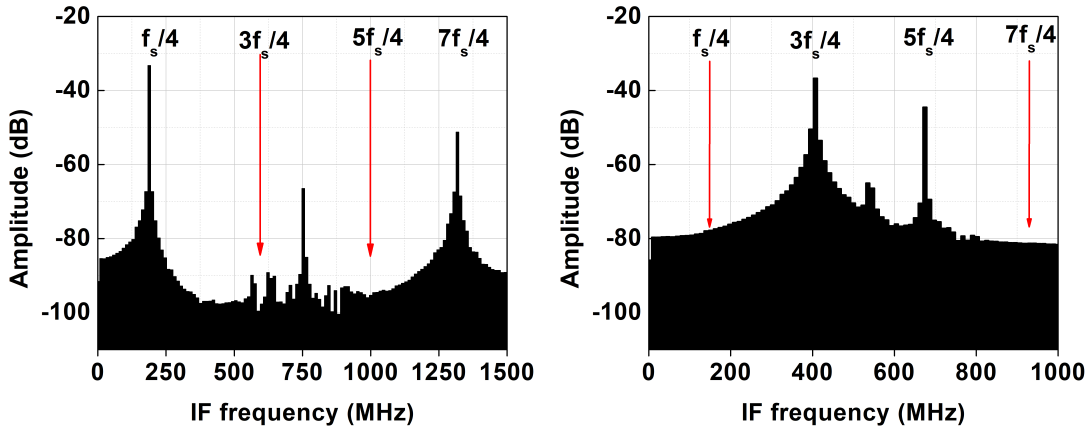
Frequency Plan

The Eq. (2.6) represents both the in-phase and quadrature outputs of the four-phase down-conversion mixer after the harmonic rejection. However, the selection of sampling frequency for a k value in Eq. (2.2) decides the rejection of particular harmonic(s). A frequency plan to select the f_s out of all possible k for a four-path sub-sampling mixer is given by Eq. (2.7).

$$f_{IF,I/Q} = \begin{cases} \frac{f_s}{4}, \frac{7f_s}{4}, .. & \text{k = 1,2,5,6,9,10,..} \\ \frac{3f_s}{4}, \frac{5f_s}{4}, .. & \text{k = 3,4,7,8,11,12,..} \end{cases} \tag{2.7}$$

To verify the frequency plan, frequency domain simulations are performed on both the single path sub-sampling mixer and four-path mixer for two sampling frequencies 752 MHz, and 537 MHz for k = 2, 3, respectively, for an input RF frequency of 940 MHz. The frequency spectrum of the single path mixer contains all the harmonics for both sampling frequencies for k = 2, 3 as shown in Fig. 2.4(a). On the other hand, the four-path mixer rejects the IF harmonics $3f_s/4$ and $5f_s/4$ for k = 2, as shown in Fig. 2.6(a), and the fundamental at $f_s/4$ and IF harmonics $7f_s/4$ are rejected for k = 3, as shown in Fig. 2.6(b).

Therefore, the proposed frequency plan of Eq. (2.7) gives the location of IF harmonics after harmonic rejection for all possible k values of f_s. In the case of a single path sub-sampling down-conversion mixer, all the IF frequencies present at the mixer output, hence, the harmonic blockers present at IF harmonic frequencies $3f_s/4$, $5f_s/4$ degrade the performance in terms of linearity and noise figure. However, the proposed harmonic rejection multi-path sub-sampling down-conversion mixer rejects the odd harmonics $3f_s/4$,



(a) (b)

Figure 2.6: Four path mixer IF output spectrum (a) for an f_{RF} of 940 MHz and f_s of 752 MHz (k = 2), and (b) for an f_{RF} of 940 MHz and f_s of 537 MHz (k = 3).

$5f_s/4$ and hence it has better linearity and noise figure. The next IF harmonic present is far from $f_s/4$, that is at $7f_s/4$, which is separated by $1.5f_s$.

2.2.3 Conversion Gain

The conversion gain of the down-conversion mixer is defined as the ratio of the output IF signal voltage to the input RF signal voltage. The single-path switch-capacitor mixer consists of the tracking output and holding outputs depending on the clock. In addition, the output spectrum of a switch-capacitor sampling mixer is a summation of the number of frequency-translated and filtered input spectra, and the equation for mixer output is given by Eq. (2.8)[48].

$$V_{IF}(f_{IF}) = \sum_{n=-\infty}^{\infty} H_n(f_{IF})\, V_{RF}(f_{RF} - nf_s) \tag{2.8}$$

where f_s is the mixer sampling frequency, $H_n(f_{IF})$ are the harmonic transfer functions(HTFs) for n^{th} harmonic, and f_{IF} is the IF frequency at the output of the mixer, and f_{RF} is the input RF frequency.

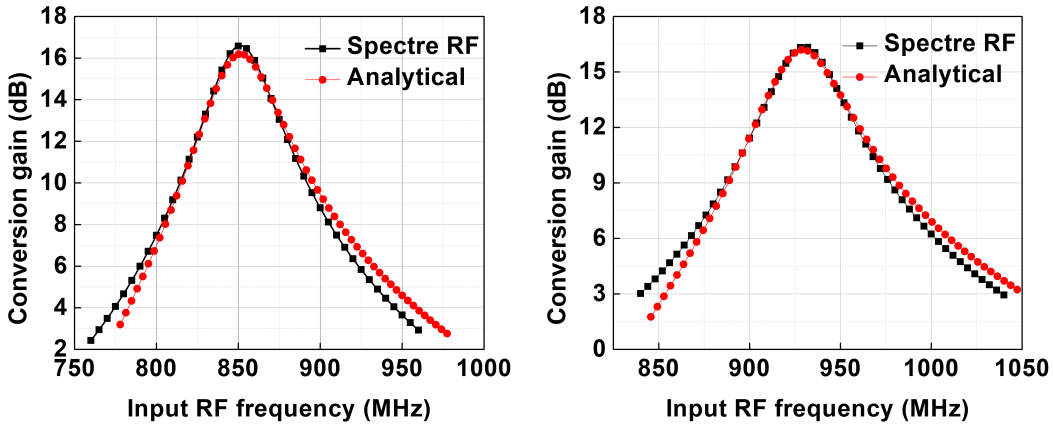
Therefore, the HTF at n^{th} harmonic represents the conversion gain of the mixer for the corresponding nf_s down-conversion. Harmonic transfer function (HTF) for the

sampling mixer is given by Eq. (2.9)[47].

$$H_n(f'_{IF}) \approx \frac{1}{1+j\frac{f'_{IF}}{f_{rc'}}}\Bigg[D \cdot sinc(Dn) \cdot e^{-j\pi Dn} + (1-D) \times \frac{sinc((1-D)f'_{IF})}{1+j\frac{f_{IF'-n}}{f_{rc'}}} e^{-j\pi(1-D)f'_{IF}} e^{-j2\pi Dn}\Bigg] \tag{2.9}$$

where $f'_{IF} = f_{IF}/f_s$, $f'_{rc} = B_{eff}/f_s$ and $B_{eff} = 1/2\pi RC$, R is the sum of switch on resistance R_{on} and source resistance R_s. For an f_{RF} of 940 MHz and f_s of 752 MHz the required down-converted IF is at $f_s/4$ of 188 MHz. For n = -1, and the duty cycle (D) = 25%, the value of HTF is 878 m(V/V). The HTF for n = -1 is the conversion gain at $f_s/4$, which is equal to -1.1 dB. Similarly, the conversion gain equation of a four-path mixer is also derived from the single-path mixer conversion gain equation by considering the respective phase shifts in the sampling clock of each path. After performing the operations ($V_{IF,I+}(t)$ - $V_{IF,I-}(t)$) and ($V_{IF,Q+}(t)$ - $V_{IF,Q-}(t)$) respectively, the conversion gain H_{n4p} of the four-path mixer becomes $2H_n$ for n =1,3,5,·· given by Eq. (2.10).

$$H_{n4p}(f_{IF}) = \begin{cases} 2H_n(f_{IF}), & \text{n = 1,3,5,··} \\ 0, & \text{n = 2,4,6,··} \end{cases} \tag{2.10}$$



(a) (b)

Figure 2.7: RF front-end conversion gain (a) for an f_s of 688 MHz and f_{RF} of 860 MHz and (b) for an f_s of 752 MHz and f_{RF} of 940 MHz.

In the proposed sub-sampling mixer-first RF front-end, the M-phase switch-capacitor bandpass filter is connected in shunt at the input of IF-LNA as shown in Fig. 1.10. The noise-cancelling inverter-based resistive feedback LNA is designed to provide a gain of 17 dB, and the estimated conversion gain of the front-end is 16.5 dB. To verify the conversion

gain of the proposed sub-sampling mixer-first RF front-end, spectreRF simulations PSS and PXF are performed for the example LR-WN standard front-end at an RF frequency of 860 MHz, sampling frequency of 688 MHz. The simulated conversion gain of the front-end is 16.5 dB, shown in Fig. 2.7(a). Similarly, the conversion gain at an RF frequency of 940 MHz and for the sampling frequency of 752 MHz is equal to 16.5 dB as shown in Fig. 2.7(b).

2.2.4 Noise Figure

The output noise power density of a single path sampling mixer is equal to the conversion gain times of the input noise power density, given by Eq. (2.11)[47].

$$N_{IF}\left(f_{IF}\right) = \sum_{n=-\infty}^{\infty} \left|H_n\left(f_{IF}\right)\right|^2 N_{RF}\left(f_{RF} - nf_s\right) \tag{2.11}$$

where N_{IF}, N_{RF}: noise power spectral density of the mixer at the output and input, respectively. Eq. (2.11) accounts for circuit-added noise from R_{on} and noise folding from all the harmonics present at the IF. It means that the single-path mixer suffers from a high noise figure. On the other hand, the HTF of the four-path mixer, given by Eq. (2.10), shows that the HTFs of rejected harmonics become zero, and the required harmonic gets amplified by two. Therefore, the improved conversion gain leads to a 3 dB decrease in the noise figure of the four-path mixer compared to a single-path mixer. The noise factor of the proposed four-path sub-sampling is obtained by substituting the Eq. (2.10) in Eq. (2.4), and it is given by Eq. (2.12).

$$F_{w4p}(IF) = \left(1 + \frac{R_{on}}{R_s}\right) \cdot \frac{\sum_{n=-\infty}^{+\infty} |H_{n4p}(f_{IF})|^2}{|H_{w4p}(IF)|^2} \tag{2.12}$$

where $H_{w4p}(f_{IF})$ is the conversion gain of the desired IF after harmonic rejection.

To verify the analysis presented above, PSS and PNOISE simulations are performed for an f_s of 752 MHz, which results in a noise figure of 4.5 dB for the four-path sub-sampling mixer, whereas it is 7.5 dB for single path mixer. Thus, it is concluded that the multi-path implementation improved the noise figure by 3 dB for all the possible sampling frequencies down-converts down-conversion to $f_s/4$, shown in Fig. 2.8. In addition, this switch-capacitor multi-path sub-sampling mixer implementation is re-configurable by the sampling frequency f_s. The total noise figure of the RF front-end, including the LNA and

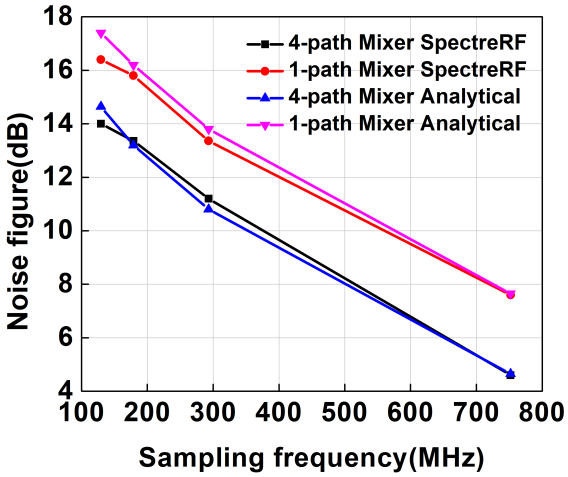


Figure 2.8: Noise figure of a single path and four path mixer for different sampling frequencies for $f_{RF} = 940$ MHz.

switch-capacitor filter, is 6.5 dB at an f_s of 752 MHz.

2.2.5 Linearity

The linearity of the proposed mixer-first sub-sampling RF front-end architecture is investigated by a two-tone test. Spectre RF QPSS and QPAC simulations are performed at the LR-WN standard frequencies of 941 MHz, 951 MHz and for a sampling frequency of 752 MHz resulting in an IIP_3 of +10 dBm. In addition, the P1dB performance of the proposed sub-sampling is investigated by performing compression test for an f_{RF} of 940 MHz and f_s of 752 MHz and for an f_{RF} of 860 MHz and f_s of 688 MHz, resulting a P1dB of +0.3 dBm, -0.3 dBm, respectively, shown Fig. 2.10(a), (b).

2.2.6 Harmonic Rejection in the Presence of Mismatches

The amount of harmonic rejection is defined as the ratio of the amplitude of the $3f_s/4$ harmonic after rejection to the $f_s/4$ amplitude. The harmonic down-conversion to $3f_s/4$ gets perfectly rejected if there are no mismatches in each path of the multi-path mixer and there is no overlapping between the non-overlapping clock. However, it is difficult to achieve 100% matching between switch-on resistance and sampling capacitance in the layout implementation leading the degradation in the harmonic rejection. To quantify the harmonic rejection, mismatches in the switch on resistance(ΔR_{on}) and sampling

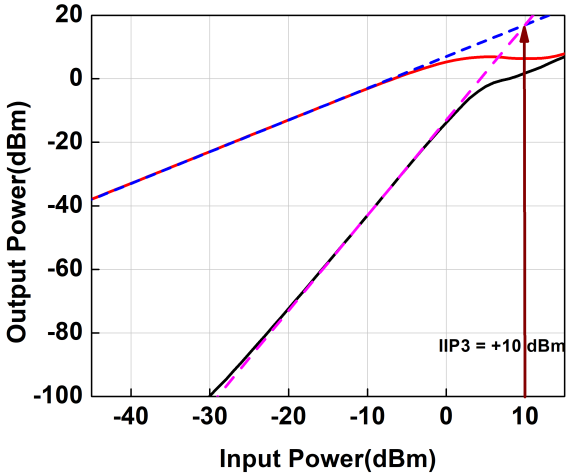
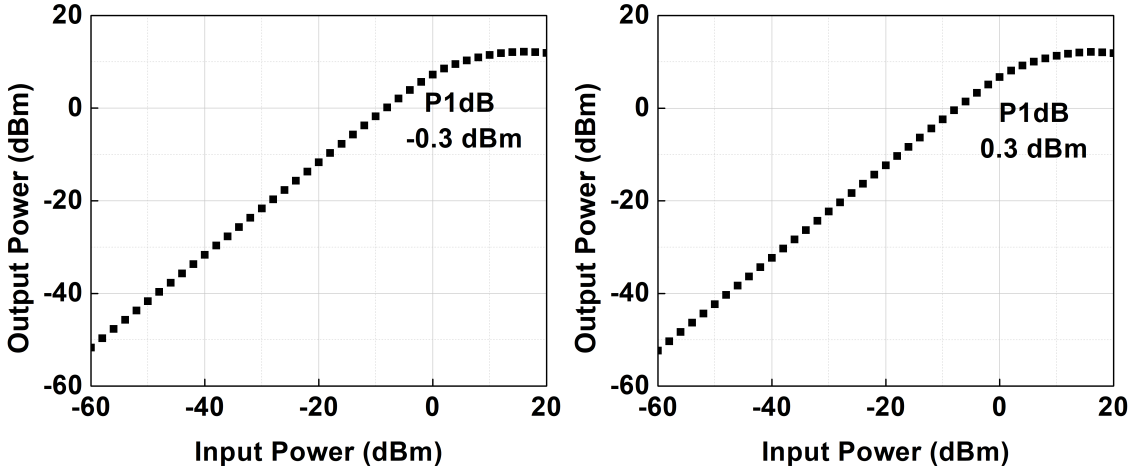


Figure 2.9: IIP_3 of the proposed RF front-end for an f_{RF} of 860 MHz, the second tone is at a 10 MHz offset and f_s of 688 MHz

capacitance(ΔC) are introduced in the harmonic transfer function (HTF) of each path. For 1% mismatch, the achievable harmonic rejection is 50 dB, and it is degraded by approx. 30 dB for a mismatch of $\pm$ 25 % of ΔR_{on} and ΔC, shown in Fig. 2.11. In addition, to generate precise 25% duty cycle non-overlapping clock phases, a D-latch-based frequency divider with division factor two is used as given in [13]. However, to estimate the degradation of harmonic rejection, a 2% of phase overlap is introduced in the clock phases, and it is found that the harmonic rejection deteriorated by less than 2 dB.

2.3 A Scheme for Sub-Sampling Mixer-First RF Front-End Input Impedance Matching

The multi-path switch-capacitor mixer transparency facilitates tunable impedance matching at the RF port by varying IF port impedance without any additional matching network at the input[13]. In an N-path mixer topology, each switch is clocked by a $(1/N)$% duty cycle clock of frequency f_s. In one period of $1/f_s$, the input port sees all the N impedances present at the output, which means the IF port impedance gets frequency translated to f_s at the RF port. Therefore, by exploiting this property, it is possible to match the input impedance of a direct down-conversion receiver to the required 50 Ω impedance since $f_{RF} \approx f_s$. On the other hand, the sampling frequency $f_s < f_{RF}$ for the sub-sampling down conversion mixer, therefore, the input impedance matching is tuned to f_s, not to the required f_{RF}. To address this issue, this work proposes an IF-stage



(a) (b)

Figure 2.10: P1dB of the RF front-end (a) for an f_s of 688 MHz and f_{RF} of 860 MHz and (b) for an f_s of 752 MHz and f_{RF} of 940 MHz.

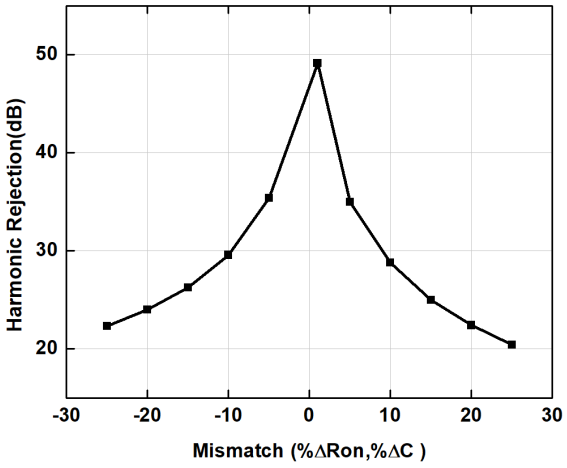


Figure 2.11: Harmonic rejection versus mismatches

impedance matching scheme using a combination of an M-phase switch-capacitor filter and IF-LNA, shown in Fig. 2.12. The M-phase filter provides frequency-shifted impedance at f_{IF}, such that the mixer translates the IF impedance to f_{RF} (= f_s+f_{IF}) at the RF port. An IF-LNA provides the required tuning impedance to match the RF port impedance to 50 Ω.

2.3.1 Input Impedance of M-phase Switch-Capacitor Filter and IF-LNA

The proposed IF stage impedance scheme includes M-phase switch-capacitor filter and IF-LNA, shown in Fig. 2.12. The switch-capacitor filter consists of M identical capacitors

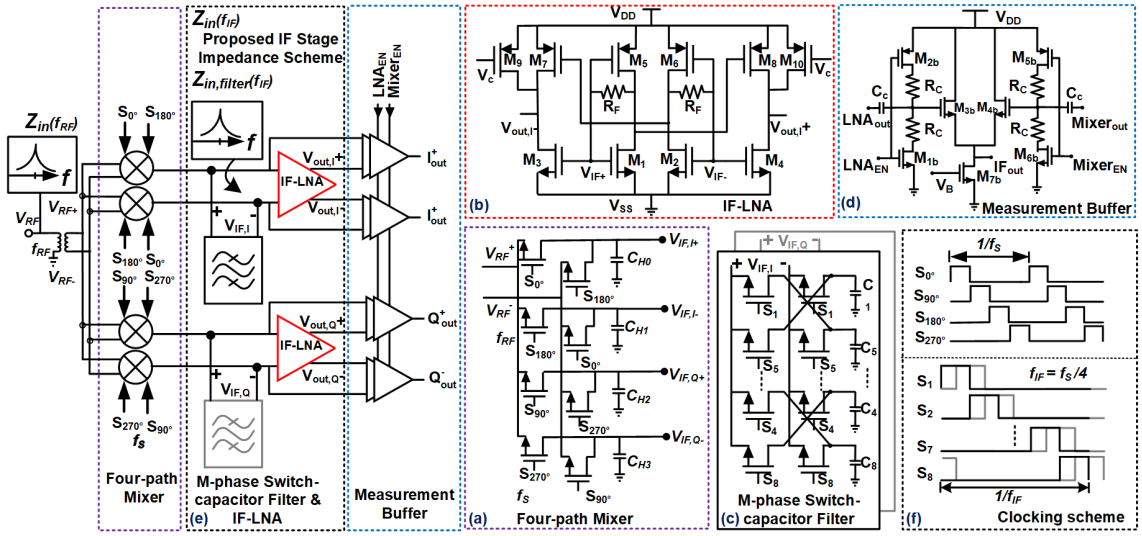


Figure 2.12: Different building blocks of the RF front-end and their circuit topologies: (a) four-path mixer (b) IF-LNA (c) M-phase switch-capacitor filter (d) measurement buffer along with (e) impedance matching scheme and (f) clocking scheme

and 2M identical switches. These 2M MOS switches are connected to M capacitors as shown in Fig. 2.12. Each M-phase filter switch is excited by $(1/M)$ duty cycle non-overlapping LOs at a frequency f_{IF}. Hence, the filter input sees two of the M capacitors over a $(1/M)^{th}$ of the period. This way, the filter impedance sees all the M-capacitors over $1/f_{IF}$ time, leading to frequency translation of low-Q impedance to a high-Q band-pass impedance centred at the frequency f_{IF}. It means that the capacitive impedance Z_C frequency translated to $Z_{in,filter}(\omega_{IF})$ at the input of the filter, and it is given by Eq. (2.13) [49].

$$Z_{in,filter}(\omega) = 2R_{sw} + 2M \sum_{n=-\infty}^{\infty} |a_{(2n+1)}|^2 Z_C(\omega - (2n+1)\omega_{IF}) \tag{2.13}$$

where the coefficient a_k is defined as $a_k = Msinc(\frac{k\pi}{M}).exp(-j\frac{k\pi}{M})$, R_{sw} is the transistor on resistance of the filter, Z_C is the impedance of the capacitor at the frequency $(\omega - (2n+1)\omega_{IF})$ for n = 0, and M represents the number of paths in the filter.

The analytical and simulated input impedance of the filter is shown in Fig. 2.13, and it is equal to 1.1 $k\Omega$ at f_{IF} frequency. Hence to match the RF port to 50 Ω antenna impedance, an inverter-based resistive feedback noise cancelling low noise amplifier is employed as shown in Fig. 2.12. The resistive feedback provides the required impedance $R_{in,LNA}$.

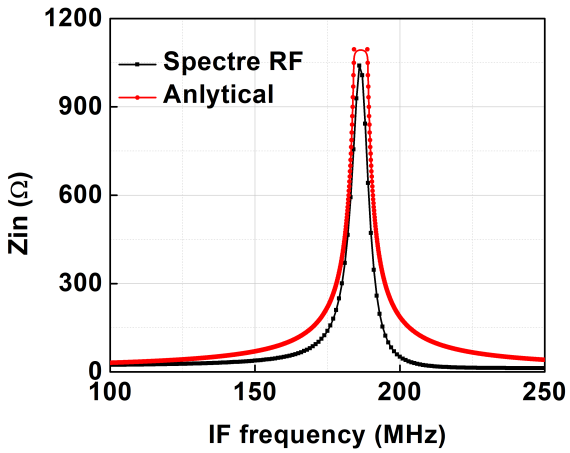


Figure 2.13: Input impedance of the IF stage switch-capacitor filter for 188 MHz sampling frequency.

2.3.2 Input Impedance of the Sub-Sampling RF Front-End

The input impedance $Z_{in}(\omega_{RF})$ of the proposed sub-sampling mixer-first RF front-end is given by Eq. (2.14) [13].

$$\begin{aligned} Z_{in}(\omega_{RF}) &= R_{on} + (\gamma Z_{in}(\omega_{IF}) \| R_{sh}) \| (\frac{1}{j\omega_{IF} C_H}) \\ &= R_{on} + \frac{\gamma\big(Z_{in,filter}(\omega_{IF}) \| R_{in,LNA}\big) \| R_{sh}}{1 + j\omega_{IF} C_H \big(\gamma(Z_{in,filter}(\omega_{IF}) \| R_{in,LNA}) \| R_{sh}\big)} \end{aligned} \tag{2.14}$$

where $Z_{in}(\omega_{IF}) = \big(Z_{in,filter}(\omega_{IF}) \| \ R_{in,LNA}\big)$, $Z_{in,filter}(\omega_{IF})$ is the input impedance of the M-phase filter given by Eq. (2.13), $R_{in,LNA}$ is the IF-LNA input impedance, and $\gamma(= \frac{2}{\pi^2})$ accounts the linear time-invariant nature of the mixer, R_{sh} represents power lost due to up-conversion by harmonics of the sampling clock through the switches to the antenna.

From Eq. (2.13), the impedance seen at the input of the filter at an f_{IF} of 188 MHz is 1.1 KΩ. In addition, the required IF stage impedance to match the 50 Ω antenna impedance is also calculated using Eq. (2.14) and realized by an IF-LNA, which is 70 Ω. To verify the proposed impedance matching scheme, the proposed RF front-end is implemented in 1.2 V, 65 nm CMOS and the Spectre RF PSS and PSP simulations are performed for both the 860 MHz and 940 MHz bands. As shown in Fig. 2.14, the input impedance of the sub-sampling mixer-first RF front-end is matched to 50 Ω for both bands.

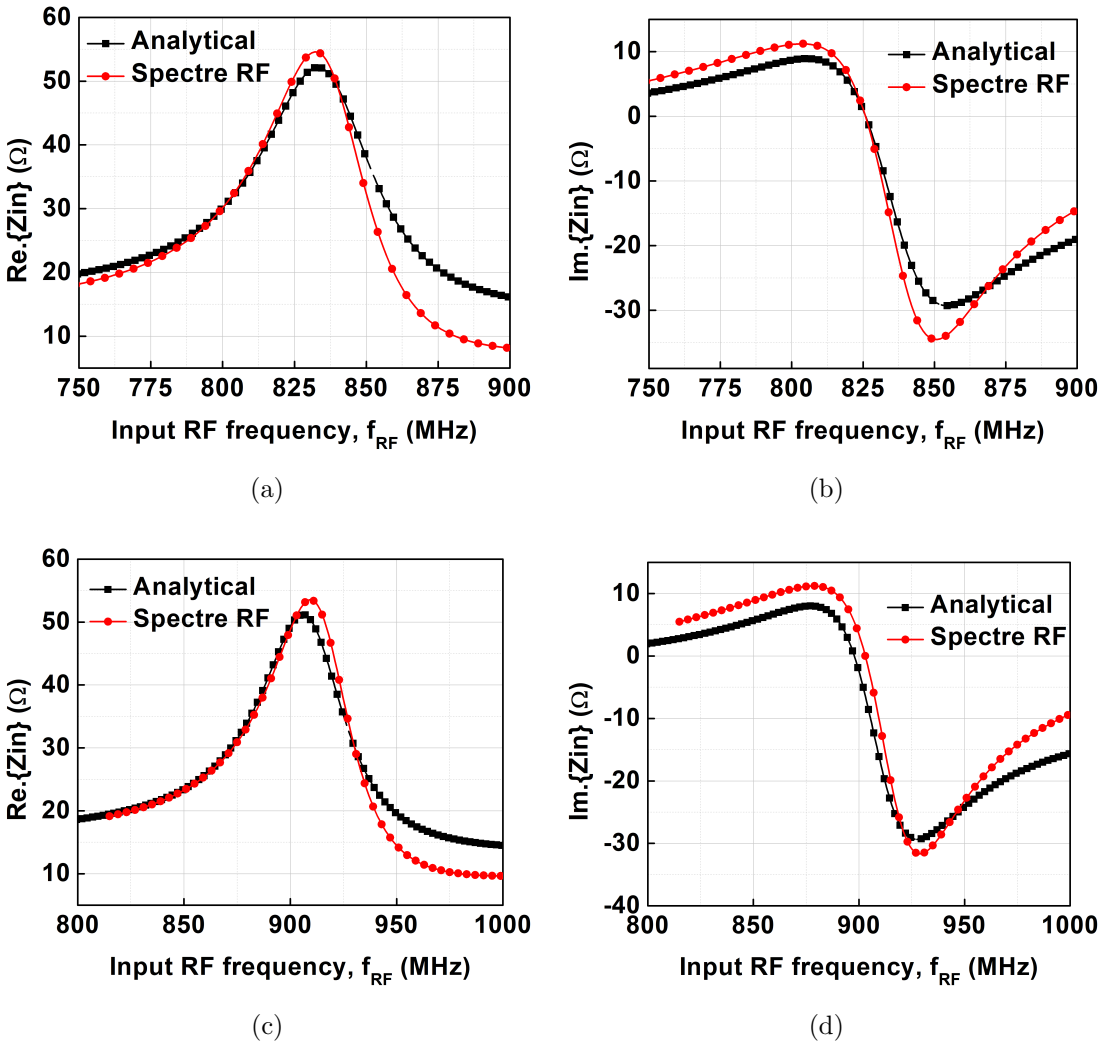


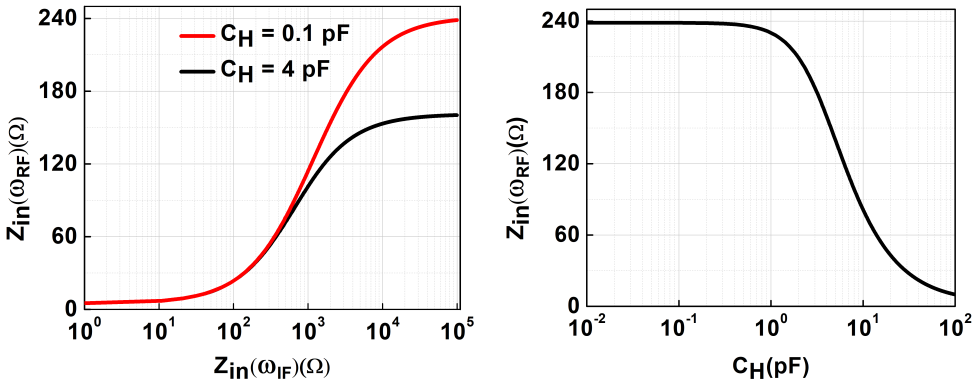
Figure 2.14: The input impedance of the sub-sampling mixer first RF front-end for an f_{RF} of 860 MHz and f_s of 688 MHz, showing the (a) real part and (b) imaginary part. Input impedance for an f_{RF} of 940 MHz and f_s of 752 MHz, showing (c) the real part (d) imaginary part

2.3.3 $Z_{in}(\omega_{IF})$ versus C_H

The input impedance given by Eq. (2.14) contains two parts: first part contains R_{on} and second part contains R_{sh}, $Z_{in}(\omega_{IF})$ and $\frac{1}{j\omega_{IF}C_H}$. Where, R_{on} is the on-resistance of the mixer switch, R_{sh} is the modelled shunt impedance, the $Z_{in}(\omega_{IF})$ is the tunable IF-stage impedance and $\frac{1}{j\omega_{IF}C_H}$ is the capacitive reactance of mixer capacitor C_H. Out of three impedances, R_{sh} a constant for a four-path passive mixer and equals to $4.3(R_S + R_{on})$[13].

Hence, the range of input impedance of the mixer depends on the parallel combination

of the two impedances, i.e., $Z_{in}(\omega_{IF})$ and $\frac{1}{j\omega_{IF}C_H}$. Generally, in the direct down-conversion mixer-first receiver, the range of input impedance is obtained by tuning the IF stage impedance, $Z_{in}(\omega_{IF})$, since the capacitive reactance is high. However, in the case of non-zero-IF down-conversion capacitive reactance also comes parallel to the $Z_{in}(\omega_{IF})$. Therefore, for the proposed RF front-end, the range of input impedance is obtained by varying one of the two, either $Z_{in}(\omega_{IF})$ or $\frac{1}{j\omega_{IF}C_H}$ at a time while keeping one of them to high impedance. Initially, the range of input impedance is obtained by varying $Z_{in}(\omega_{IF})$ from 1-100 kΩ while keeping f_{IF} and C_H constant at 188 MHz and 0.1 pF. This analysis shows that the mixer transparency provides a tunable impedance match with the lower limit equal to R_{on}, and the upper limit is $R_{on} + R_{sh}$ as shown in Fig. 2.15(a). However, as explained above, to find the effect of $\frac{1}{j\omega_{IF}C_H}$ on input impedance, the C_H is set to 4 pF which resulted in a reduced upper limit as shown in Fig. 2.15(a). To identify the upper limit of the input impedance, $Z_{in}(\omega_{IF})$ versus C_H analysis is performed by varying C_H from 0.01-100 pF using Eq. (2.14) for an f_{IF} of 188 MHz, $Z_{in}(\omega_{IF})$ of 100 kΩ. The input impedance obtained from this analysis is shown in Fig. 2.15(b). The input impedance ranges from 5 Ω to 240 Ω, and it is greater than 50 Ω for C_H <11 pF. Hence, in the proposed scheme, selecting a sampling capacitor of less than or equal to 11 pF facilitates 50 Ω matching by varying IF stage impedance. This analysis shows that selecting a suitable C_H is essential in realizing input impedance matching for non-zero-IF down-conversion mixers.



(a) (b)

Figure 2.15: Input impedance of the front-end from Eq. (2.14)(a) $|Z_{in}(\omega_{RF})|$ for varying IF stage impedance $|Z_{in}(\omega_{IF})|$, (b)$|Z_{in}(\omega_{RF})|$ for varying C_H.

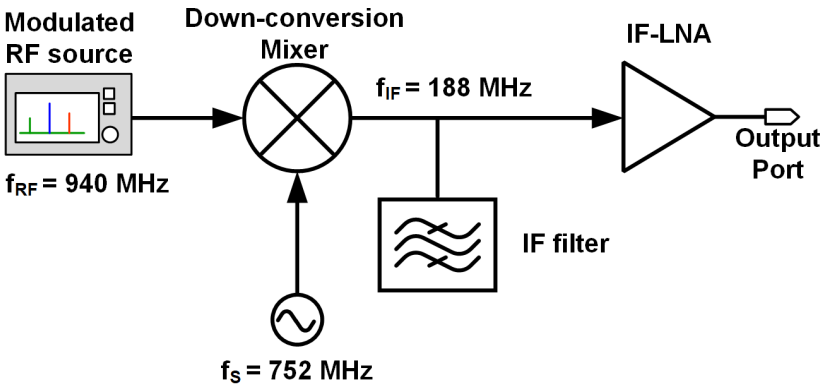


Figure 2.16: Block diagram of the proposed sub-sampling mixer-first RF front-end for EVM simulation.

Table 2.2: Block-level specification of the proposed receiver RF front-end for system-level EVM simulation

Parameter	Mixer	IF-LNA	IF filter
Noise Figure(dB)	4	1.8 to 10	NA
Gain(dB)	-1.1	6 to 18	-0.6
IIP_3(dBm)	+16	-1 to 3	NA

2.4 System Level Error Vector Magnitude(EVM) performance

The system-level error vector magnitude(EVM) simulations are performed for the RF front-end by using Genesys model shown in Fig. 2.16 for the block-level specifications given in Table. 2.2.

The RF front-end model consists of a down-conversion mixer, IF stage switch-capacitor filter, and IF LNA. The input to the mixer is an M-array-based RF modulated 16-QAM source. The simulated EVM at the output of the LNA is shown in Fig. 2.17. The EVM is limited by the noise at low input signal powers and the RF front-end linearity at the higher input signal power levels. In addition, the EVM of the receiver is also verified for three gain settings of IF-LNA from 6 to 18 dB with a sampling clock jitter of 600 fs. The target EVM of -30 dB is achieved for an input signal power range from -80 to 0 dBm as shown in Fig. 2.17.

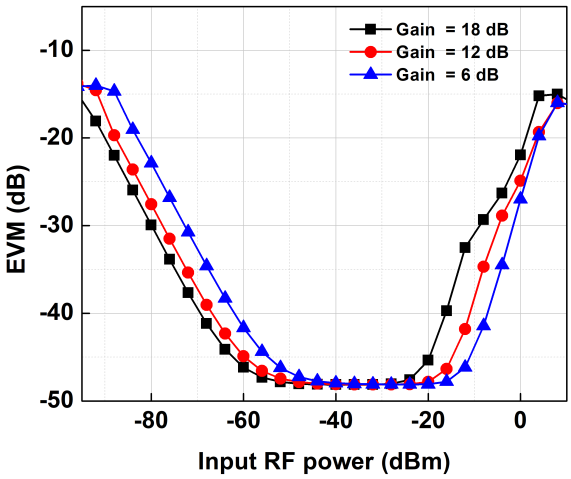


Figure 2.17: System level EVM of the complete RF front-end for varying input power levels and gain of the IF-LNA.

Table 2.3: Performance summary of the proposed RF front-end

		Sampling Scheme	Architecture	Impedance matching w/o LNA	Supply(V)	Area(mm^2)		
		Sub-sampling	Mixer-first	Yes	1.2/2.5	0.32		
f_{RF}(GHz)	f_s(GHz)	NF(dB)	BW(MHz)	IIP_3(dBm)	Gain(dB)	Power(mW)		
						Mixer +filter	LO	IF/BB
0.4-1	0.32-0.8	6.5-8	50	+10	16	0.4	6-12.6	23

2.5 Conclusion

An architecture for process scalable low noise figure impedance matched sub-sampling mixer-first RF front-end is presented, and the performance summary is given in Table. 2.3. It has been demonstrated the feasibility of such an architecture through analytical equations and by spectre RF simulations addressing the core issues such as high noise figure and lack of impedance matching as needed in mixer-first RF front-end with an example low power RF front-end in 1.2 V, 65 nm CMOS for wideband operation from 0.4-1 GHz, specifically for two bands at f_{RF} of 860 MHz and 940 MHz.

However, the proposed sub-sampling RF front-end is a non zero-IF kind and hence needs an additional IF-stage impedance scheme for achieving impedance matching since the sampling frequency is not an integer multiple of f_s. Therefore, to achieve impedance matching without an additional network at RF or IF/BB a presents the digitally intensive sub-sampling mixer-first direct down-conversion RF front-end is proposed and the idea is presented in Chapter 3.

Chapter 3

Digitally Intensive Sub-Sampling Mixer-First Direct Down-Conversion RF Font-End

This chapter presents the proposed digitally intensive sub-sampling mixer-first direct down-conversion RF front-end architecture. Section 3.1 explains the introduction of the sub-sampling direct down-conversion receiver, including the trade-off between power consumption versus operating frequency of the clock generation circuits based on the recently published architectures. Section 3.2 explains the scheme of sub-sampling direct down-conversion eight-path mixer implementation, and the performance analysis of the proposed RF front-end is also presented as explained in Section 1.5.2. Section 3.3 presents the impedance matching scheme for sub-sampling mixer-first direct down-conversion receiver architecture and noise figure, conversion gain and IIP_3. The EVM analysis of the proposed RF front-end is presented in Section 3.4, and Section 3.5 concludes the chapter.

3.1 Sub-sampling Direct Down-conversion Mixer-First RF Front-End Architecture

This section presents the sub-sampling down-conversion low power paradigm and the architecture of the proposed quarter-rate sub-sampling direct down-conversion mixer-first RF front-end. In addition, the frequency plan, eight-path sub-sampling direct down-conversion mixer, and harmonic recombination schemes are explained. Moreover, the performance analysis of the proposed RF front-end in terms of conversion gain, noise figure, and linearity is presented.

3.1.1 Sub-Sampling Down-Conversion: A Low-Power Paradigm

The advancements in the technology scaling improved the switching performance of the transistor; hence, the switch-capacitor RF front-ends circuits, such as passive N-path mixers and N-path filters, offer re-configurable operation over a wide frequency range.

However, extending the operation to higher RF frequencies leads to an increase in the overall power budget of the receiver due to the rapid increase in power consumption of the frequency synthesizer, non-overlapping multi-phase clock generation and distribution circuitry. Sampling-based N-path receivers [10, 12, 32–35] employ clock dividers to generate precise multi-phase non-overlapping clocks. These dividers require a clock frequency of $Nf_s/2$ for generating non-overlapping clocks with a frequency, f_s. Therefore, the power consumption of multi-phase non-overlapping clock generation and distribution in RF sampling-based receivers is no longer negligible, as shown in Fig. 3.1.

The power consumption of the clocking circuit surpasses the receiver chain power consumption as the operating frequency increases[10, 12, 32–35]; hence, it limits the frequency range of operation. On the other hand, implementing the down-conversion using a sub-sampling mixer requires a sampling frequency less than the input RF frequency, hence offering a solution to the power consumption issue[10]. Supporting this statement, Fig. 2.1(b) shows the power consumption of frequency generation circuits with respect to the operating RF frequency[36–43]. It is evident from Fig. 2.1(b) that as the sampling frequency of a mixer reduces, the power consumption of the clocking circuitry reduces significantly.

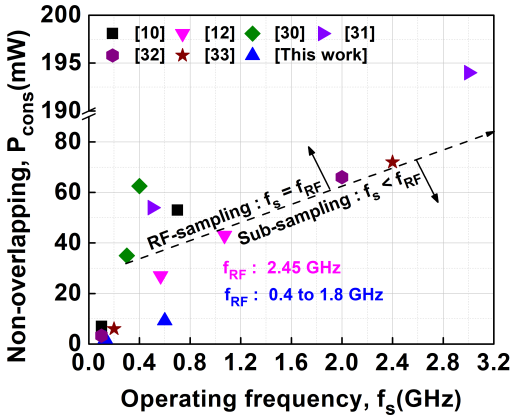


Figure 3.1: Power consumption of the non-overlapping clock generation circuits

In addition, a recent work[3] on lower power bounds for clock generation circuits also emphasized the impact of increased power consumption at higher operating frequencies of wireless and wireline communication systems. The voltage-controlled oscillator (VCO) power consumption grows with the square of the clock frequency, f_s, specifically, the $P_{VCO} \propto f_s^2$. This trend of increased power consumption makes it challenging to design clock generation at a higher frequency of operation for low-power applications. How-

ever, sub-sampling down-conversion requires a sampling frequency less than the input RF frequency, reducing the clock generation's power budget.

$$P_{VCO,RF} \propto f_{s,RF}^2 = f_{RF}^2 \tag{3.1a}$$

$$P_{VCO,SS} \propto f_{s,SS}^2 = \left(\frac{4f_{RF}}{2k+1}\right)^2 \tag{3.1b}$$

$$P_{VCO,QRSS} \propto f_{s,QRSS}^2 = \left(\frac{f_{RF}}{2k+1}\right)^2 \tag{3.1c}$$

For a given f_{RF}, the power consumption of VCOs for the RF sampling down-conversion($P_{VCO,RF}$), sub-sampling ($P_{VCO,SS}$) and quarter-rate sub-sampling($P_{VCO,QRSS}$) is given by Eq. (3.1a), (3.1b), and (3.1c), respectively. The ratio of power consumption of the VCOs for both the sub-sampling down-conversion techniques is normalized with the $P_{VCO,RF}$ and shown in Fig. 3.2. For a given RF, compared with the RF sampling, the sub-sampling down-conversion technique and quarter-rate sub-sampling technique save the power of the VCO by more than 36% and 89%, respectively. Therefore, sub-sampling down-conversion receiver architectures offer a solution to reduce the power budget of the clock generation and distribution circuits.

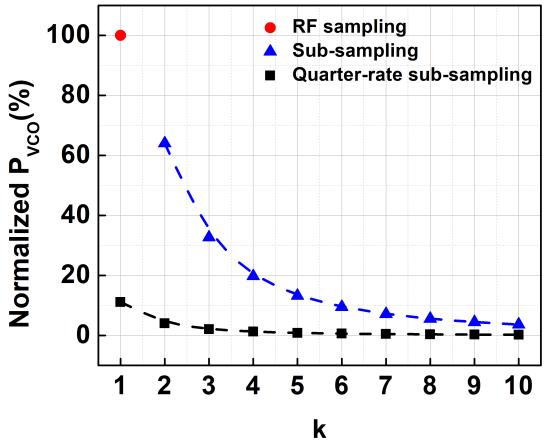


Figure 3.2: Comparison of VCO power consumption with respect to RF sampling, sub-sampling, and quarter-rate sub-sampling

3.2 Quarter-Rate Sub-Sampling Direct Down-Conversion Architecture

The block diagram of the proposed quarter-rate sub-sampling mixer-first receiver RF front-end architecture is shown in Fig. 3.3. The major contributions of the proposed work are one, sub-sampling direct down-conversion eight-path mixer scheme and two, impedance

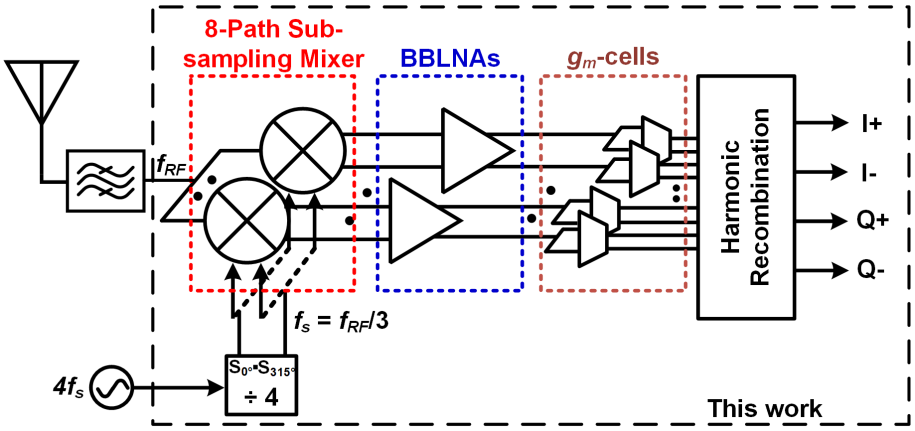


Figure 3.3: Block diagram of the proposed quarter-rate sub-sampling direct down-conversion mixer-first RF front-end

matching at the RF front-end of the mixer, using the third harmonic of the sampling frequency (f_s). The RF front-end employs an eight-path quarter-rate sub-sampling direct down-conversion mixer, which translates the input RF signal to a zero-IF. The translated baseband signal gets amplified by the baseband low noise amplifiers (BBLNA's). In addition, the BBLNA provides the required base-band impedance, which is translated to the RF port of the mixer to match 50 Ω antenna impedance. The BBLNA outputs are further amplified and duplicated by g_m-cells. The g_m-cell outputs are recombined to obtain the third harmonic quadrature down-conversion and to attenuate the fundamental and fifth harmonic down-conversions. The major blocks of the proposed RF front-end are implemented with process scalable components such as switches, capacitors and inverters, making the RF front-end a digitally intensive architecture.

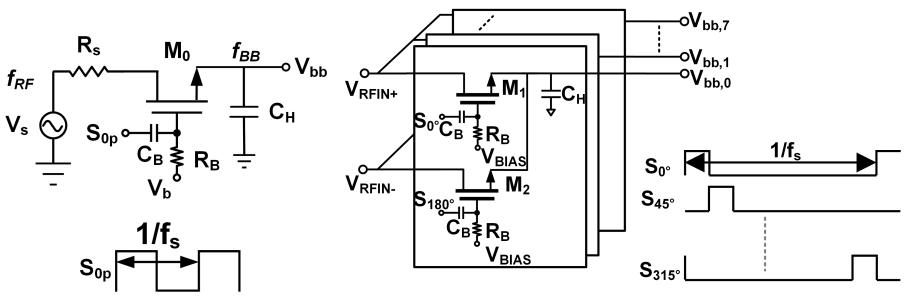
3.2.1 Frequency Plan

In sub-sampling down-conversion, for a given input RF signal with frequency f_{RF}, the sampling frequency F_s is selected from Eq. (3.2a), and the IF outputs are generated at odd harmonics of $F_s/4$[7].

$$\left.\begin{aligned} F_s &= \frac{4f_{RF}}{2k+1}; k = 0, 1, 2, 3 \ldots \\ f_{IF} &= \min\left(|f_{RF} - nF_s|\right) = F_s/4 \end{aligned}\right\} \tag{3.2a}$$

$$\left.\begin{aligned} f_s = F_s/4 = \frac{f_{RF}}{2k+1} \\ f_{BB} = f_{RF} - nf_s; n = 1, 3, 5 \ldots \end{aligned}\right\} \tag{3.2b}$$

As explained in Section 2.2, a single-path switch-capacitor mixer, shown in Fig. 3.4(a), serves the purpose of sub-sampling down-conversion; however, it has a high noise figure, does not provide quadrature direct down-conversion and impedance matching[9]. On the other hand, an N-path sub-sampling down-conversion mixer approach using F_s offers a low noise figure, quadrature down-conversion and impedance matching[28]. However, the down-conversion is to a non-zero IF, and the effective sampling frequency, $f_{s,eff}$ of the N-path approach increases to NF_s. Therefore, to reduce the effective sampling frequency of N-path implementation and to achieve direct down-conversion to zero-IF, this work employs an eight-path mixer with the third harmonic of the quarter-rate sub-sampling frequency, f_s given by Eq. (3.2b). Where, f_{BB} is baseband frequency, f_{IF} is intermediate frequency, and n represents the harmonic of f_s. Thus, the proposed architecture deploys a unique sub-sampling scheme compared to RF sampling for realizing the direct down-conversion and saving on the clocking circuitry power consumption.



(a) (b)

Figure 3.4: (a) Single path switch-capacitor mixer, (b) eight path sub-sampling mixer and non-overlapping clocking scheme with 12.5% duty cycle[29]

3.2.2 Eight-Path Direct Down-Conversion Mixer and Harmonic Recombination Scheme

The eight-path switch-capacitor sub-sampling mixer is shown in Fig. 3.4(b). Each path of the mixer is excited by quarter-rate sub-sampling frequency, f_s with 12.5% duty-cycle non-overlapping clocks, S_{0° to S_{315°. The down-converted baseband output voltage on the capacitor of m^{th} path of the mixer is denoted by $V_{bb,m}$ and it is calculated by solving

the charge balance equation given by Eq. (3.3)[50].

$$Q_m = \frac{V_{bb,m}}{f_s \times R_{BB}} = \int_{m/8f_s - 1/16f_s}^{(m+1)/8f_s - 1/16f_s} \frac{V_{RF} - V_{bb,m}}{R_{sw}} dt \tag{3.3}$$

The solution for $V_{bb,m}$ for V_{RF} = A $\cos(\omega_{RF}t + \phi)$ is given by Eq. (3.4), where $\omega_{RF} = n\omega_s$ and $n = 1, 3, 5, \cdot\cdot$

$$V_{bb,m} = \frac{8R_{BB}}{(R_{BB} + 8R'_s)} sinc(\frac{n\pi}{8}) A \cos\left(\frac{nm\pi}{4} + \phi\right) \tag{3.4}$$

where $R'_s = (R_s + R_{sw})$, R_s is the antenna impedance, R_{sw} is the on-resistance of the switch, and R_{BB} is the real component of base-band stage input impedance.

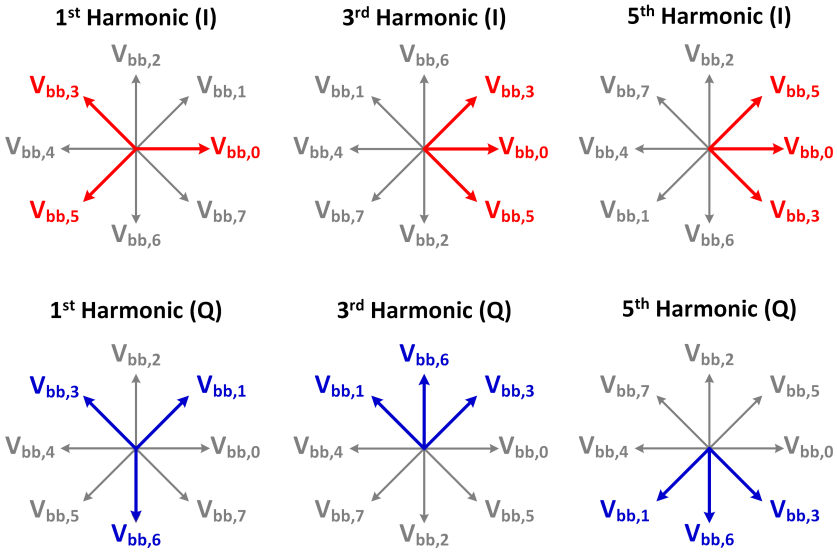
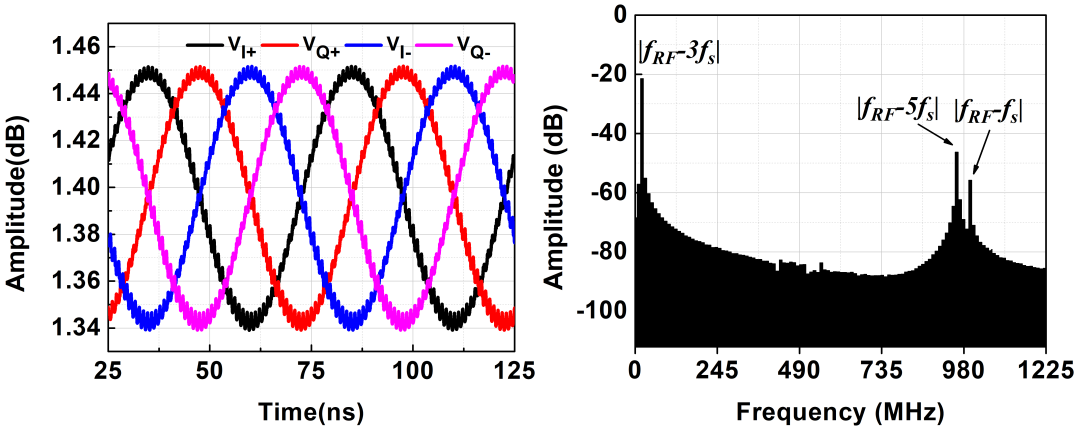


Figure 3.5: Vector representation of the baseband voltages of the eight-path mixer with respect to fundamental, 3^{rd} and 5^{th} harmonics of the sampling frequency, f_s

The eight-path mixer output voltages $V_{bb,0}$ to $V_{bb,7}$ are obtained by substituting the phase of the corresponding sampling clock in Eq. (3.4). The resultant baseband output voltages experience a phase shift of $(n \times 360/N)°$, where N = 8. It means that the eight baseband voltages corresponding to the fundamental, third and fifth harmonics of f_s experience a phase shift 45°, 135° and 225°, respectively, as shown in Fig. 3.5. Therefore, to obtain the quadrature outputs for third harmonic down-conversion, $V_{bb,0}$ to $V_{bb,7}$ are recombined as given in Eq. (3.5a) with uniform-weighing gain. The resultant simplified I and Q output expressions are given by Eq. (3.5b), for the direct down-conversion of the RF signal present at the third harmonic of f_s to the zero-IF.



(a) (b)

Figure 3.6: Proposed RF front-end (a) time domain output waveforms, and (b) in-phase output spectrum for an f_{RF} of 1490 MHz, f_s of 490 MHz

$$\left.\begin{aligned} V_I &= (V_{bb,0} + V_{bb,3} + V_{bb,5}) - (V_{bb,1} + V_{bb,4} + V_{bb,7}) \\ V_Q &= (V_{bb,1} + V_{bb,3} + V_{bb,6}) - (V_{bb,2} + V_{bb,5} + V_{bb,7}) \end{aligned}\right\} \tag{3.5a}$$

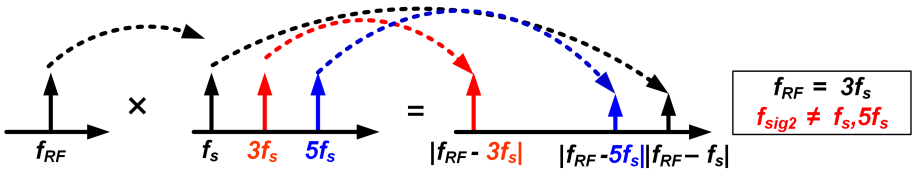
$$\left.\begin{aligned} V_I &= \frac{K}{3} A[(2+2\sqrt{2})cos\phi] \\ V_Q &= \frac{K}{3} A[(2+2\sqrt{2})sin\phi] \end{aligned}\right\} \tag{3.5b}$$

$$\left.\begin{aligned} V_I &= \begin{cases} KA[(2-2\sqrt{2})cos\phi], n = 1 \\ \frac{K}{5} A[(2+2\sqrt{2})cos\phi], n = 5 \end{cases} \\ V_Q &= \begin{cases} KA[(2-2\sqrt{2})sin\phi], n = 1 \\ \frac{K}{5} A[(2+2\sqrt{2})sin\phi], n = 5 \end{cases} \end{aligned}\right\} \tag{3.5c}$$

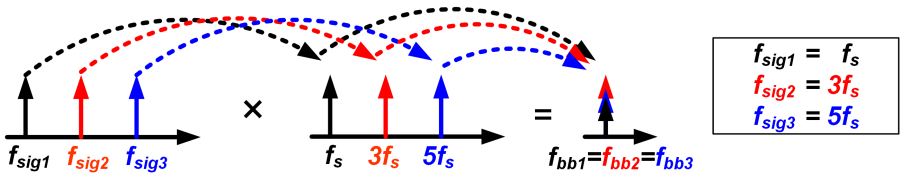
where, $K = \frac{8R_{BB}sin(\frac{n\pi}{8})}{\pi(R_{BB}+8R'_s)}$. To verify the proposed quarter-rate sub-sampling direct down-conversion scheme, time domain simulations are performed, for an f_{RF} of 1490 MHz and f_s of 490 MHz. The time domain differential quadrature base-band outputs and the frequency spectrum of the in-phase outputs are shown in Fig. 3.6(a) and Fig. 3.6(b) respectively. The frequency spectrum contains desired down-converted base-band output, $f_{RF} - 3f_s$ at 20 MHz and down-conversions from the fundamental and fifth harmonic of f_s at 1 GHz and 960 MHz, respectively as shown in Fig. 3.7(a).

3.2.3 Conversion Gain

In the proposed quarter-rate sub-sampling direct down-conversion scheme, the down-conversion is implemented by the third harmonic of f_s; hence, the conversion gain of the RF front-end is defined as the ratio of the amplitude of the signal down-converted to zero-IF to the RF signal amplitude at the $3f_s$. However, in addition to $3f_s$, it is important to know the conversion gain of the front-end for blockers present at the fundamental, f_s and fifth harmonic, $5f_s$, as these blockers are down-converted to zero-IF as shown in Fig. 3.7(b). This is quantified by $\left|\frac{V_{I/Q,(1,5)}}{V_{I/Q,3}}\right|$ using the Eq. (3.5b), and (3.5c), gives the magnitude of rejection of the blockers at f_s or $5f_s$ with respect to the desired third harmonic down-conversion. The magnitude of the attenuation for the fundamental f_s, to third harmonic $3f_s$, is 12.5 dB, and for the fifth harmonic, $5f_s$ to third harmonic, $3f_s$ is 5 dB. However, the blockers present at the fundamental and fifth harmonic of f_s are well separated with respect to $3f_s$, and they are already attenuated sufficiently by the front-end RF filters usually available in a practical RF system.



(a)



(b)

Figure 3.7: Harmonic down-conversion of the mixer (a) for signal present at the 3^{rd} harmonic of the sampling frequency, f_s, (b) for signal present at the corresponding harmonic of the sampling frequency, f_s

In the proposed quarter-rate sub-sampling RF front-end, BBLNA, g_m- cell and eight-path switch-capacitor mixer provides a voltage gain of 16 dB, 6.5 dB and -0.5 dB, respectively. To verify the conversion gain of the proposed quarter-rate sub-sampling mixer-first RF front-end, spectreRF simulations PSS and PXF are performed for an f_{RF} of 1470 MHz

and f_s of 490 MHz and for the harmonic scheme shown in Fig. 3.7(a). The simulation result shows that the conversion gain of the RF front-end for the $3f_s$ is 22 dB as shown in Fig. 3.8.

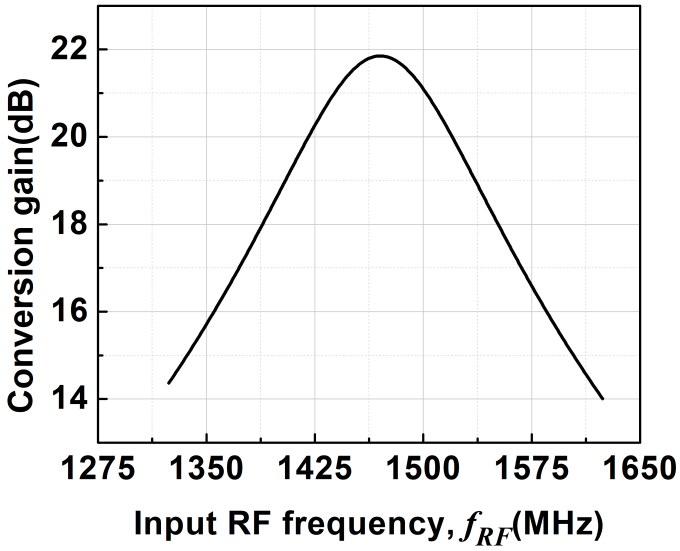


Figure 3.8: Conversion gain of the RF front-end for an f_{RF} of 1470 MHz and f_s of 490 MHz

3.2.4 Noise Figure

The equivalent noise model of the proposed RF front-end is shown in Fig. 3.9. The RF front-end contains the following major sources of noise: noise due to the resistance of the MOS switch, R_{sw}, baseband stage noise including baseband stage resistance, R_{BB} and g_m-cell. The noise figure of the RF front-end for n^{th} harmonic down-conversion is given by Eq. (3.6), which is derived based on LTV analysis given in [51, 52].

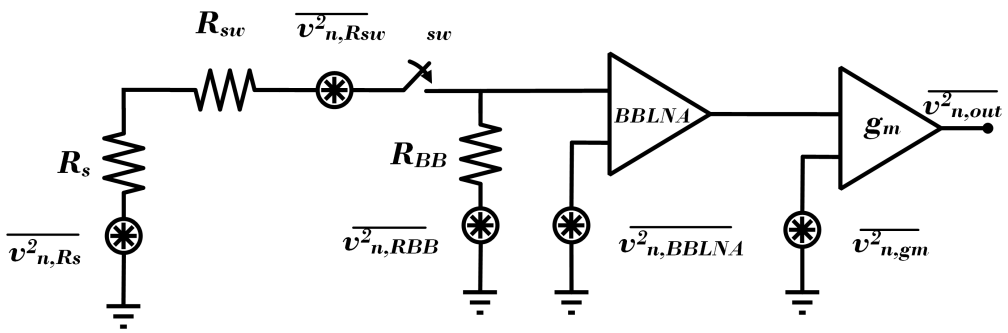


Figure 3.9: Equivalent noise model of the proposed RF front-end

$$NF(n) = \frac{1}{sinc^2(\frac{n\pi}{N})}\left(1 + \frac{R_{sw}}{R_s} + \frac{NR_s}{R_{BB}(1+A_v')}\left(1+\frac{R_{sw}}{R_s}\right)^2 + \frac{\overline{v_{n,BBLNA}^2}}{N\overline{v_{n,Rs}^2}} + \frac{\overline{v_{n,gm}^2}}{N\overline{v_{n,Rs}^2}A_{v,BBLNA}^2}\right) \tag{3.6}$$

where N is the number of mixer paths. $\overline{v_{n,R_s}^2}$, and $\overline{v_{n,R_{sw}}^2}$ are noise contributions from the source resistance, R_s and switch resistance, R_{sw}. $\overline{v_{n,BBLNA}^2}$ and $\overline{v_{n,gm}^2}$ are input referred noise of the BBLNA and gm-cell, respectively. R_{BB} is the baseband stage impedance, and A_v' is the voltage gain of the first stage of BBLNA.

The noise figure of the RF front-end, given by Eq. (3.6), shows that the noise figure increases at higher harmonics of sampling frequency f_s, even though it requires a low sampling frequency and reduces the clocking circuitry's power consumption. On the other hand, increasing the number of paths in an N-path mixing scheme offers a low noise figure for a selected harmonic down-conversion. It means that for a selected harmonic down-conversion, the eight-path mixer offers a lower noise figure than the 4-path mixer. Therefore, an eight-path mixer with quarter-rate sub-sampling third harmonic down-conversion is implemented in this work.

The noise figure of the proposed RF front-end is obtained for a R_{sw} of 10 Ω, R_{BB} of 250 Ω, $A_{v,BBLNA}$ of 16 dB, $\overline{v_{n,BBLNA}^2}$ of 0.7 nV/$\sqrt{Hz}$ and $\overline{v_{n,gm}^2}$ of 1.4 nV/$\sqrt{Hz}$ using Eq. (3.6). The obtained DSB noise figure of the RF front-end is 4.2 dB for the third harmonic down-conversion.

To verify the noise analysis presented above, spectreRF PSS and PSP simulations are performed for the proposed quarter-rate sub-sampling mixer-first RF front-end. The spectreRF simulation results show that the RF front-end, including an eight-path mixer, BBLNAs and g_m-cells has a DSB noise figure of 4.6 dB, for an f_{RF} of 1.47 GHz and an f_s of 490 MHz. From this analysis, it is evident that the quarter-rate sub-sampling architecture achieves a noise figure comparable with the RF sampling front-end.

3.2.5 Linearity and Power Consumption

SpectreRF QPSS and QPAC simulations are performed to estimate the in-band IIP_3 (IB-IIP_3) of the quarter-rate sub-sampling direct down-conversion RF front-end for two

input tones at 1.47 GHz and 1.471 GHz with 1 MHz offset, and sampling frequency of 490 MHz. The resultant IIP_3 of the proposed sub-sampling zero-IF receiver is -1 dBm, shown in Fig. 3.10. In addition, the P1dB performance of the proposed sub-sampling is investigated by performing compression test for an f_{RF} of 1470 MHz and f_s of 490 MHz and for an f_{RF} of 940 MHz and f_s of 313.3 MHz, resulting a P1dB of -15 dBm, -15 dBm, respectively, shown Fig. 3.11(a), (b). In this work, the linearity of the BBLNA is optimized to provide a -1 dBm IIP_3, which has increased the power consumption of BBLNA to 23 mW at 1.2 V supply. The detailed analysis of LNA performance optimization is provided in Section 4.1.1.3.

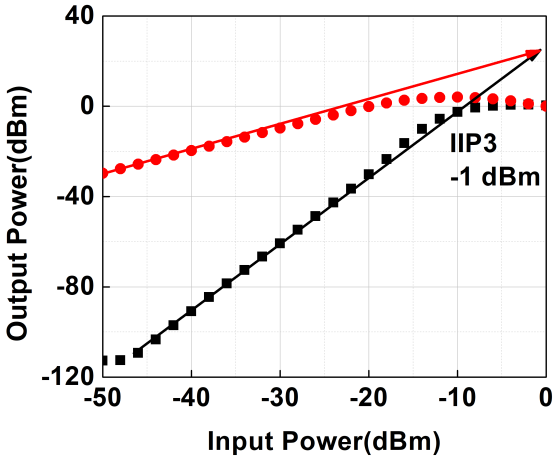


Figure 3.10: IIP_3 of the proposed RF front-end for an f_{RF} of 1470 MHz, the second tone is at a 10 MHz offset and f_s of 490 MHz

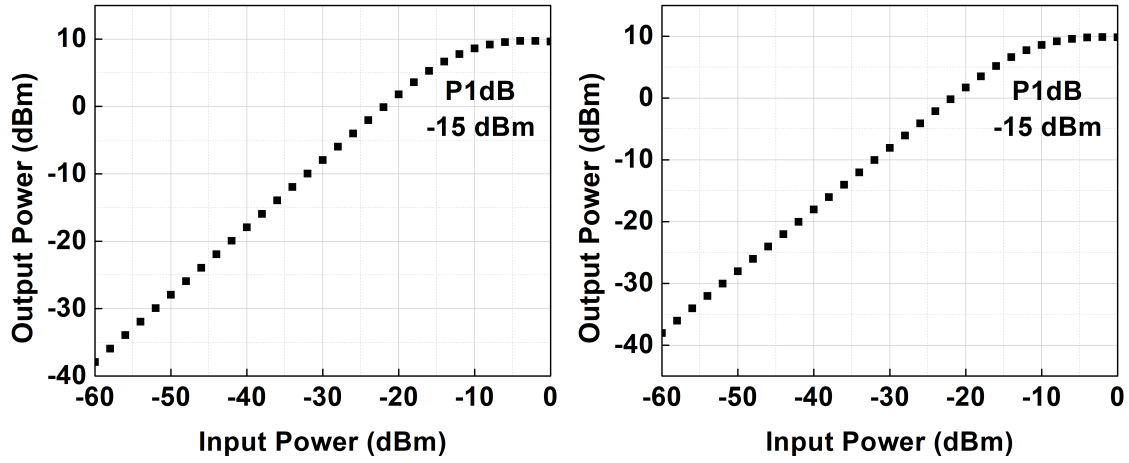


Figure 3.11: P1dB of the RF front-end (a) for an f_s of 313.3 MHz and f_{RF} of 940 MHz and (b) for an f_s of 490 MHz and f_{RF} of 1472 MHz.

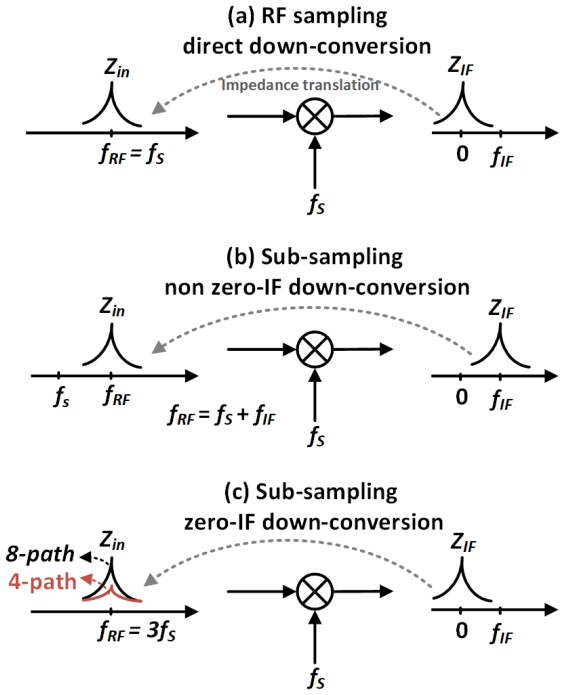


Figure 3.12: Impedance translation for (a) RF sampling zero-IF down-conversion, (b) sub-sampling non-zero-IF down-conversion, and (c) proposed sub-sampling zero-IF down-conversion

3.3 Impedance Matching Scheme

In a switch-capacitor mixer-first receiver, the passive mixer transparency facilitates the input impedance matching by frequency translating the baseband stage impedance to the RF port of the mixer[50]. In RF sampling down-conversion, each switching path of the N-path mixer conducts for $\frac{1}{N}^{th}$ of the sampling period $1/f_s$. Hence, the RF port sees baseband impedance at every instance of the sampling period, and it gets up-converted to the sampling frequency f_s at the RF port, as shown in Fig. 3.12(a). However, for the sub-sampling down-conversion, f_s is less than f_{RF}. Therefore, an additional IF stage matching scheme is required to translate the impedance to the RF port of the mixer[28] as shown in Fig. 3.12(b). On the other hand, employing the proposed sub-sampling down-conversion scheme translates baseband impedance to f_{RF} using the third harmonic of quarter-rate sub-sampling frequency as shown in Fig. 3.12(c). Therefore, the proposed scheme eliminates the need for an additional IF-stage impedance matching network for sub-sampling down-conversion receivers.

The equivalent model of differential N-path mixer is represented by the linear time-

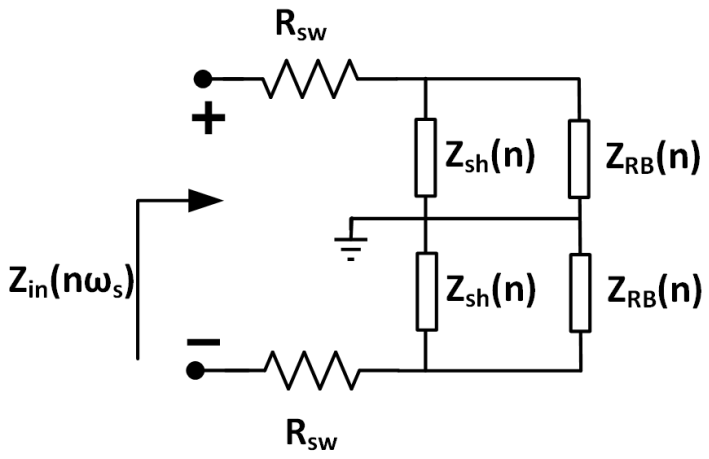


Figure 3.13: Input impedance model for differential N-path mixer[29]

invariant (LTI) model as shown in Fig. 3.13. The equivalent input impedance at the RF port of the mixer for nth harmonic of the sampling frequency is given by Eq (3.7)[50, 51].

$$\left.\begin{aligned} Z_{in}(n\omega_s) &= 2R_{\text{sw}} + 2(Z_{sh}(n) \parallel Z_{RB}(n)) \\ Z_{RB}(n) &= \frac{1}{N}\ sinc^2\left(\frac{n\pi}{N}\right)\left(R_{in,BBLNA} \parallel \frac{1}{j\omega_{BB}C_H}\right) \\ Z_{sh}(n) &= \frac{sinc^2(\frac{n\pi}{N})}{1 - sinc^2(\frac{n\pi}{N})}(R_s + R_{sw}) \end{aligned}\right\} \tag{3.7}$$

where Z_{RB} represents up-converted baseband impedance and Z_{sh} represents the folding shunt impedance at n^{th} harmonic, $R_{in,BBLNA}$ represents the input impedance of the BBLNA, and C_H is the sampling capacitor of the mixer. It is evident from Eq. (3.7) that the baseband impedance is frequency translated to switching frequency 'f_s' and its harmonics. However, as the 'n' increases, Z_{sh} decreases, and if it becomes less than 50 Ω, it is not possible to match the antenna impedance. For the four-path mixer, the Z_{sh} is less than 50 Ω at all the harmonics other than fundamental frequency f_s. Hence, 50 Ω impedance matching is only possible at the fundamental, f_s. On the other hand, increasing the number of paths to eight, the magnitude of the shunt impedance Z_{sh} surpasses 50 Ω for the fundamental and third harmonic of f_s. This property of the eight-path mixer allows matching the input impedance at the fundamental and third harmonic of f_s by tuning baseband impedance $R_{in,BBLNA}$. Therefore, an eight-path sub-sampling switch-capacitor mixer is employed for realizing impedance matching using the third harmonic of f_s.

SpectreRF PSS, PSP simulations are performed to validate the input impedance

obtained from the analytical equations. In the proposed quarter-rate sub-sampling mixer-first receiver architecture, the BBLNA provides the required baseband impedance to match 50 Ω at the RF port of the mixer. The simulated real and imaginary components of the input impedance are shown in Fig. 3.14(a) and Fig. 3.14(b) for an f_{RF} of 1.476 GHz, f_s = 492 MHz, respectively. The input return loss, S_{11}, simulations shown in Fig. 3.14(c) confirms that the input impedance matches to 50 Ω at the third harmonic of f_s and poor matching at the fundamental and fifth harmonics of f_s.

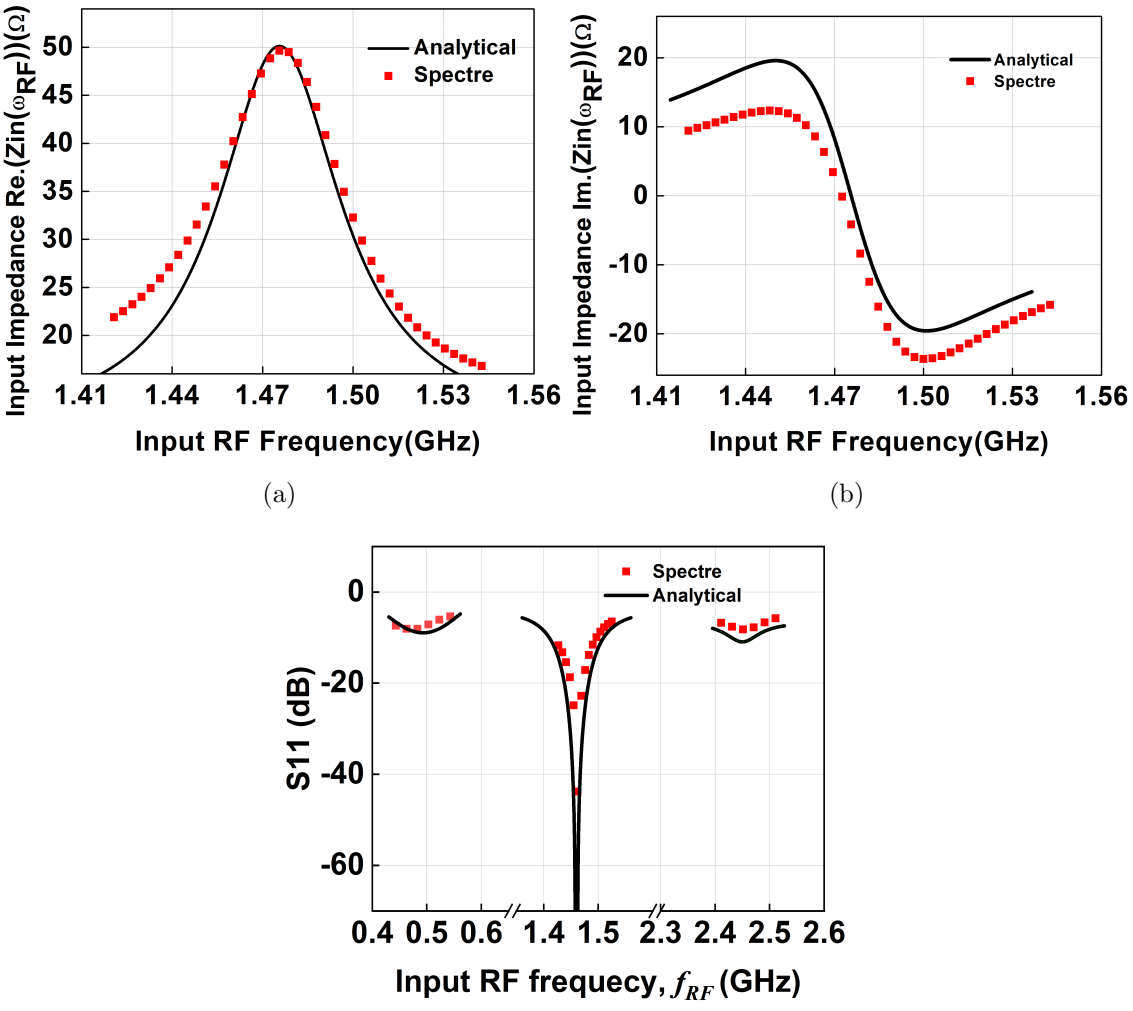


Figure 3.14: The input impedance of the sub-sampling mixer-first direct down-conversion RF front-end for an f_{RF} of 1470 MHz and f_s of 490 MHz, showing the (a) real part, (b) imaginary part and (c) S_{11}

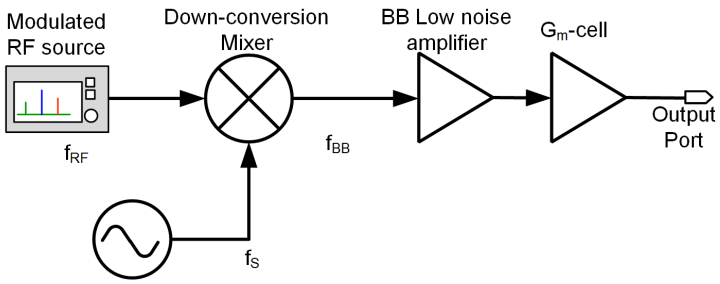


Figure 3.15: Block level model of the RF front-end

Table 3.1: Block level specifications of the proposed sub-sampling direct down-conversion receiver

Parameter	Mixer	BBLNA	Gm-cell
Noise Figure(dB)	3*	1.8 to 12	9.4
Gain(dB)	0.4	6 to 18	8
IIP_3(dBm)	+13.9	-1.1 to 12	+2.6

* NFDSB

3.4 System Level Error Vector Magnitude(EVM) Analysis

In general, the performance of an RF system is presented in terms of different parameters such as noise figure, IIP_3, signal-to-noise ratio, etc., Similarly, error vector magnitude is a metric which gives a combined impact of different impairments such as noise, non-linearity. The system-level EVM analysis of the proposed sub-sampling mixer-first direct down-conversion RF front-end is performed by using a Genesys model, shown in Fig. 3.15. The sub-sampling RF front-end consists of a mixer, BBLNA, followed by a g_m-cell. The block-level specifications used for the EVM simulations are given in Table. 3.1. The input to the mixer is an M-array-based RF modulated 16-QAM source and the simulated EVM at the output of the BBLNA. The simulated EVM of the RF front-end is shown in Fig. 3.16 for varying input power from -100 dBm to +20 dBm. The EVM becomes poor for the input power less than -90 dBm and greater than 0 dBm, which means that the performance of the RF front-end is limited by the noise at low input signal powers and the RF front-end linearity at the higher input signal power levels. In addition, the EVM of the receiver is also verified for three gain settings of BBLNA from 6 to 18 dB with a sampling clock jitter of 600 fs. The RF front-end achieves a target EVM of -30 dB or better for an input range of -80 dBm to -20 dBm input power.

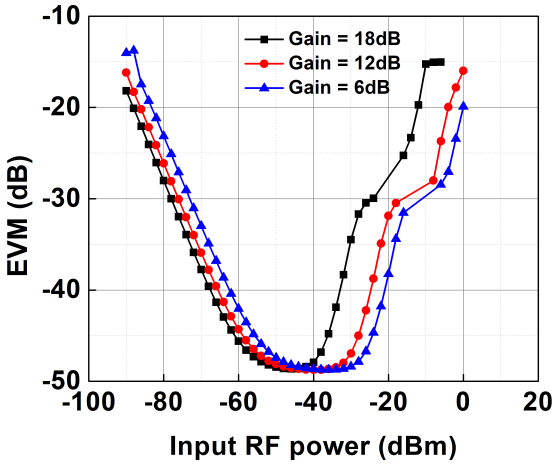


Figure 3.16: System level EVM of the RF front-end for varying input RF power and BBLNA gain

Table 3.2: Performance summary of the proposed RF front-end

		Sampling Scheme	Architecture	Impedance matching w/o LNA	Supply(V)	Area(mm^2)		
		Sub-sampling	Mixer-first	Yes	1.2/2.5	0.32		
f_{RF}(GHz)	f_s(GHz)	NF(dB)	BW(MHz)	IIP_3(dBm)	Gain(dB)	Power(mW)		
						Mixer	LO	BB
0.4-1.8	0.13-0.6	7.5-8	50	-1	22	0.8	2-10	25

3.5 Conclusions

A digitally intensive sub-sampling direct down-conversion mixer-first receiver architecture has been presented. The concept of sub-sampling direct down-conversion and the input impedance matching scheme at the RF port of the mixer using the third harmonic of the f_s is explained. The scheme of the proposed architecture is demonstrated using analytical equations and spectreRF simulations and summary of performance is given in Table. 3.2. The proposed receiver architecture is realized in the 1.2 V, 65 nm CMOS process with the circuit components like switches, capacitors and inverters makes it digitally intensive architecture. The required sampling frequency for the proposed architecture is one-third of the input RF frequency, leading to low power consumption for the clock generation. These features make the proposed architecture a potential candidate for low-power applications.

The CMOS implementation details of both the proposed sub-sampling RF front-ends are provided in Chapter 4.

Chapter 4

CMOS Implementation of Sub-Sampling RF Front-end Architectures

This chapter provides CMOS implementation details of the two digitally intensive sub-sampling mixer-first RF front-ends presented in Chapters 2 and 3. Initially, in section 4.1, circuit and layout implementation details of each sub-block of the first sub-sampling mixer-first RF front-end, along with the non-overlapping clocking scheme and post-layout performance summary, are provided. After that, in Section 4.2, circuit and layout implementation details of each sub-block of the second RF front-end, along with the non-overlapping scheme and post-layout performance summary, are presented. In Section 4.3, the details of the full-chip layout, input, output pin specifications, and placement details of all the sub-blocks are presented. Finally, section 4.4 concludes the chapter.

4.1 A Process Scalable Architecture for Low Noise Figure Sub-Sampling Mixer-First RF Front-End

The proposed sub-sampling RF front-end is implemented in 1.2 V, 65 nm CMOS technology. As shown in Fig. 2.12, the proposed sub-sampling mixer-first RF front-end consists of a four-path sub-sampling mixer, IF stage switch-capacitor filters, and IF-LNAs. The four-path mixer down-converts the incoming RF signal to IF and also offers harmonic rejection leading to a low noise figure. The IF-LNA in combination with the switch-capacitor filter offers the required gain at IF and impedance matching at the RF port. The impedance realized by this combination at the IF stage is frequency translated to RF by exploiting the transparency property of the passive mixer.

4.1.1 Circuit Implementation

This section explains the circuit implementation details of the proposed sub-sampling mixer-first architecture along with the non-overlapping clock generation scheme. Block

and circuit level implementation of the proposed RF front-end is shown in Fig. 2.12.

4.1.1.1 Four-Path Sub-Sampling Mixer

As explained in Section 1.2, in the advanced CMOS technologies, the switching properties of the MOS transistors have been improved[6]; hence MOS switches are commonly employed in switch-capacitor implementations [5]. In this work, a four-path sub-sampling mixer is employed for down-conversion. As shown in Fig. 2.12 (a), the differential four-path mixer consists of four switching paths, and each path is excited by four 25% duty cycle non-overlapping clocks S_{0°, S_{90°, S_{180° and S_{270°. Each path of the mixer conducts for one-fourth of the sampling period and samples the input RF signal onto four capacitors C_{H0} to C_{H3}. These four outputs are in quadrature and denoted by $V_{IF,I+}$, $V_{IF,I-}$, $V_{IF,Q+}$ and $V_{IF,Q-}$.

4.1.1.2 IF-LNA

The CMOS inverter-based amplifiers exhibit good noise figure, gain, and linearity performance, along with the advantage of process scalability. In this work, an IF-LNA is employed to provide the required impedance at the IF port of the mixer using a CMOS inverter-based resistive feedback wide-band amplifier as shown in Fig. 2.12(b). The transconductance G_m of the first stage of IF-LNA is the sum of both g_{mN} and g_{mP} offers a better gain. In addition, it provides noise cancellation at the output node leading to a low noise figure. The gain of the IF-LNA is given by Eq. (4.1).

$$\begin{aligned} A_v &= \left(A_{v'} \times g_{m7,8} + g_{m3,4}\right)\left(r_{o3,4} \| r_{o7,8}\right) \\ &\text{Where} \\ A_{v'} &= \frac{1 - G_m R_F}{1 + \frac{R_F}{R_o}}; G_m = g_{m1,2} + g_{m5,6} \end{aligned} \tag{4.1}$$

The input impedance of the IF-LNA is denoted as $R_{in,LNA}$ and the analytical equation is given by Eq. (4.2). The feedback resistor R_F and voltage gain are designed to get the required input impedance at the IF stage. The total impedance at the IF stage of the RF front-end is the parallel combination of $R_{in,LNA}$ of IF-LNA and the input impedance of the IF stage filter. As it will be explained in Section 4.1.1.3, the input impedance of the

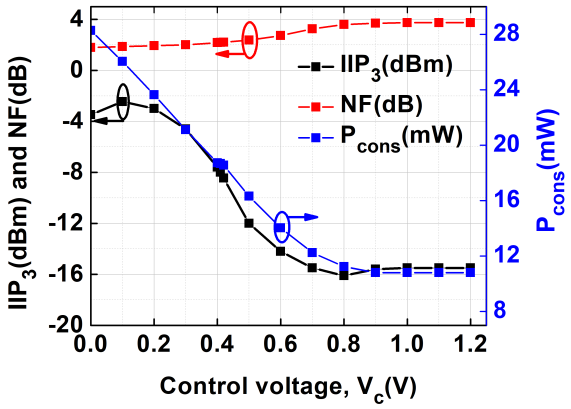


Figure 4.1: IIP_3, noise figure and power consumption of the IF-LNA with respect to control voltage V_c.

IF stage filter is high; hence, the input impedance of IF-LNA is tuned to match the RF port impedance of the mixer to 50 Ω antenna impedance.

$$R_{in,LNA} = 2\left(\frac{R_F + R_o}{1 + G_m R_o}\right)$$
$$R_o = r_{o5,6} \| r_{o1,2} \tag{4.2}$$

In the proposed work, the IIP_3 of the switch-capacitor RF front-end is limited by the IF-LNA linearity. Hence, the IF-LNA performance is optimized to provide an IIP_3 of -2.4 dBm, which increases the power consumption of the IF-LNA. The control voltage V_c is applied to the IF-LNA, as shown in Fig. 2.12 (b), to set the required performance and power consumption. The performance of the IF-LNA for varying V_c is shown in Fig. 4.1. It shows increasing V_c reduces the power consumption of the IF-LNA; however, this affects the linearity of the RF front-end.

4.1.1.3 M-Phase Switch-Capacitor Filter

The M-phase switch-capacitor bandpass filter consists of M number of replicas of the switch-capacitor low-pass filter. These switches are excited by M-phase non-overlapping clocks where each path conducts $\frac{1}{M}^{th}$ period of the clock. The switching creates a bandpass impedance response at the input of the filter by exploiting the transparency property of passive switch capacitors [49]. In this work, an eight-phase filter is implemented to create a bandpass impedance response at the input of the filter. The differential 8-phase switch-

capacitor consists of sixteen MOS switches and eight capacitors as shown in Fig. 2.12 (c). These switches are excited by eight non-overlapping clock phases S_1 to S_8 with a sampling frequency of f_{IF}. The switching creates a bandpass impedance response centred at f_{IF}, which facilitates the impedance matching for the proposed RF front-end at f_{RF}. The filter bandwidth depends on the sampling capacitors, which provide tunable bandwidth by varying the capacitance.

4.1.1.4 Measurement Buffer

The circuit diagram of the measurement buffer is shown in Fig. 2.12(d). The buffer is designed to measure both the mixer and IF-LNA outputs separately with the help of two control signals, LNA_{EN} and $Mixer_{EN}$. Based on the selection of control signals, the buffer gives one of the two signal inputs LNA_{out}, $Mixer_{out}$ to IF_{out} output. In this work, the measurement buffer is designed using 2.5 V supply transistors and provides an IIP_3 of 32 dBm, -1.6 dB loss, consumes a 3 mA current and has a 50 Ω impedance at the output. The buffer with such high linearity eliminates the need for de-embedding the buffer non-linearity in the measurements.

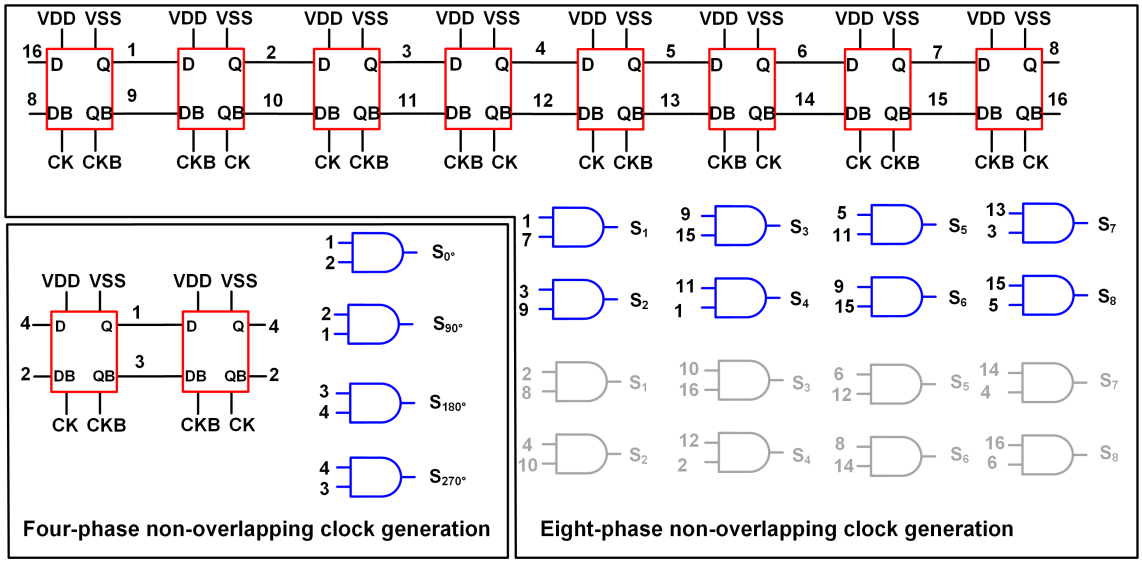


Figure 4.2: Four and eight phase non-overlapping clock scheme

4.1.1.5 Non-Overlapping Clock Generator

The four and eight-phase non-overlapping clocks with 25% and 12.5 % duty cycles are generated using two frequency dividers from the same input source[13, 49]. An on-

chip single-to-differential converter is employed to convert the external single-ended clock to a differential clock. These differential clock phases are divided by latch-based clock dividers, and the divider output phases are combined using combinational logic to generate non-overlapping clock phases with the required duty cycle[13]. Fig. 4.2 shows the non-overlapping clock scheme for the proposed RF front-end. The 8-phase clock for the Q-path filter is delayed by 90° to avoid discharging of Q-path sampling capacitors when the S_{90°, and S_{270° phases are OFF.

4.1.2 Layout Implementation

The proposed sub-sampling RF front-end is implemented in the 1.2 V, 65 nm CMOS technology and the full custom layout is implemented for the test chip. This section provides the post-layout performance summary of each block of the proposed RF front-end.

4.1.2.1 Layout of the Switch-Capacitor Four-Path Mixer

The layout of the differential four-path sub-sampling switch-capacitor mixer is shown in Fig. 4.3. As explained in Section 4.1.1.1, the differential input RF signal RF_{IN+}, RF_{IN-}, and the four-phase non-overlapping clocks S_{0°, S_{90°, S_{180° and S_{270° are applied to the mixer at the marked positions in the layout. The down-converted IQ outputs V_{I+}, V_{I-}, V_{Q+} and,V_{Q-} are obtained across the four sampling capacitors as shown in Fig. 4.3.

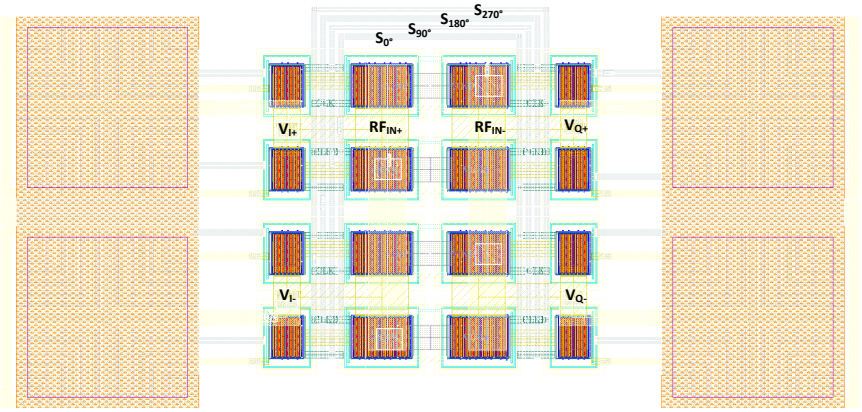


Figure 4.3: Layout of the four-path switch-capacitor mixer

4.1.2.2 Layout of the IF-LNA

Two CMOS inverter-based differential IF-LNA are employed in the proposed architecture as shown in Fig. 2.12. The two differential quadrature outputs of the sub-sampling mixer are connected to the LNAs. These LNAs give the IF outputs of the sub-sampling RF front-end with a gain of 16 dB. The decoupling capacitors are used for biasing the IF-LNA independently which increases the area of the LNA. The layout of the IF-LNA, excluding decoupling capacitors, is shown in Fig. 4.4.

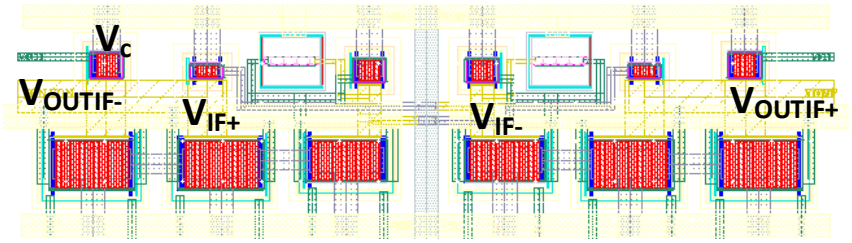


Figure 4.4: Layout of the IF-LNA

4.1.2.3 Layout of the M-Path Filter

As explained in Section 4.1.1.3, the proposed switch-capacitor filter consists of eight differential switch paths and eight capacitors. The differential quadrature outputs of the four-path mixer are the input to both the filters in the architecture. The eight outputs of the filter switches are connected to eight capacitors. The inputs of the filter are denoted as V_{IF+} and V_{IF-}. The layout of the M-phase switch-capacitor band-pass filter is shown in Fig. 4.5.

4.1.2.4 Layout of the Non-Overlapping Clock Generation

As shown in Fig. 2.12, the proposed RF front-end architecture requires two non-overlapping clocking schemes. The four-phase clock for sub-sampling down-conversion mixer and an eight-phase clock generation circuit for M-phase switch-capacitor filters. The reference clock to these two non-overlapping clock generation circuits is provided

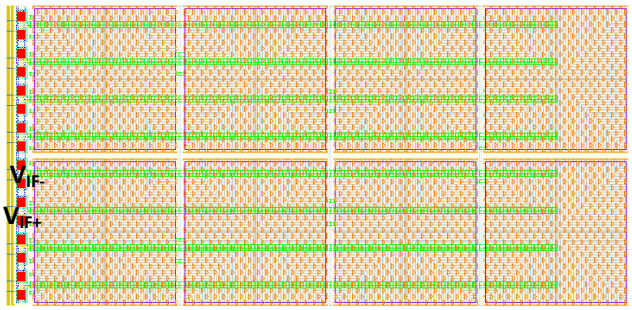
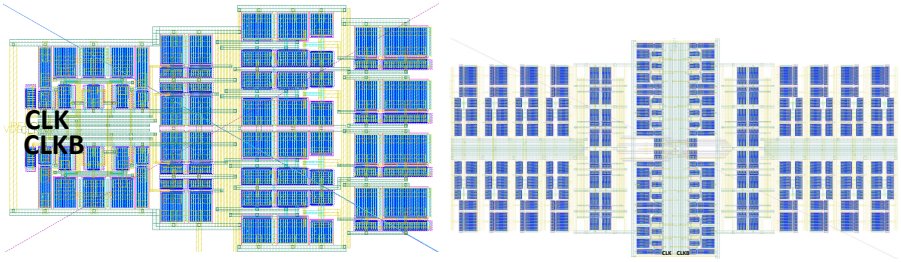


Figure 4.5: Layout of the M-path filter

externally. The two inputs CLK and CLKB are generated by a single-ended to the differential converter and the differential outputs are connected simultaneously to both the four-phase and eight-phase non-overlapping clock generation signals as shown in Fig. 4.6(a) and 4.6(b). The outputs of both the clock generation circuits are connected to the mixer and filter switches using clock buffers.



(a) (b)

Figure 4.6: Layout of the (a) four-phase non-overlapping clock generator and (b) eight-phase clock generator.

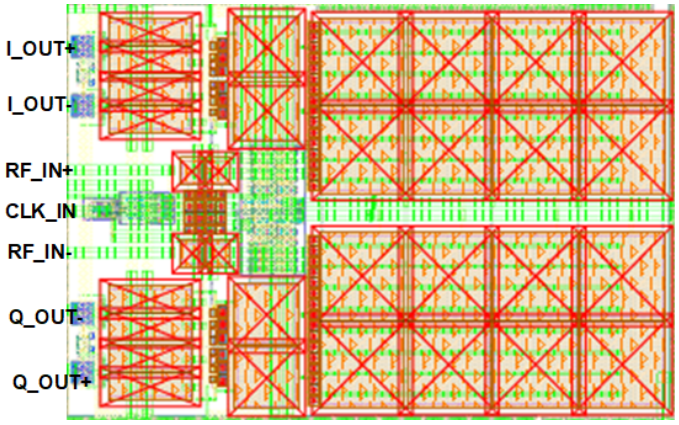


Figure 4.7: Layout of the full architecture

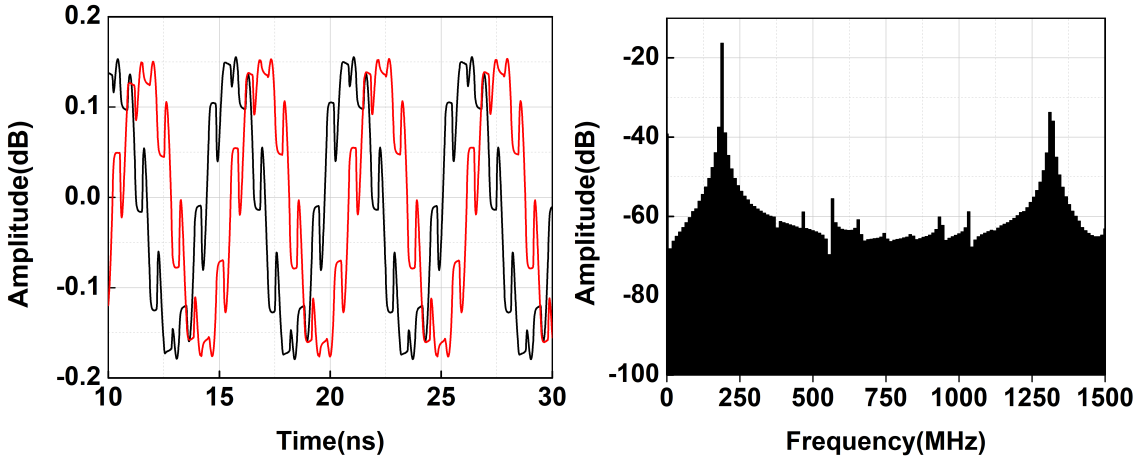
4.1.3 Post-Layout Performance

The full custom layout architecture of the proposed architecture is implemented, shown in Fig. 4.7. The post-layout performance of the proposed process scalable low noise figure sub-sampling mixer-first receiver RF front-end is simulated, and the results are provided below.

4.1.3.1 Transient Simulation

The transient response of the proposed RF front-end is simulated at an RF frequency of 860 MHz and a sampling frequency of 688 GHz. The simulated time domain and frequency spectrum of the IF outputs are shown in Fig. 4.8(a) and 4.8(b) respectively. The transient outputs shown in Fig. 4.16(a) are in quadrature, and the spectrum of the in-phase output shown in Fig. 4.16(b) confirms the down-conversion to an IF frequency of $f_s/4$.

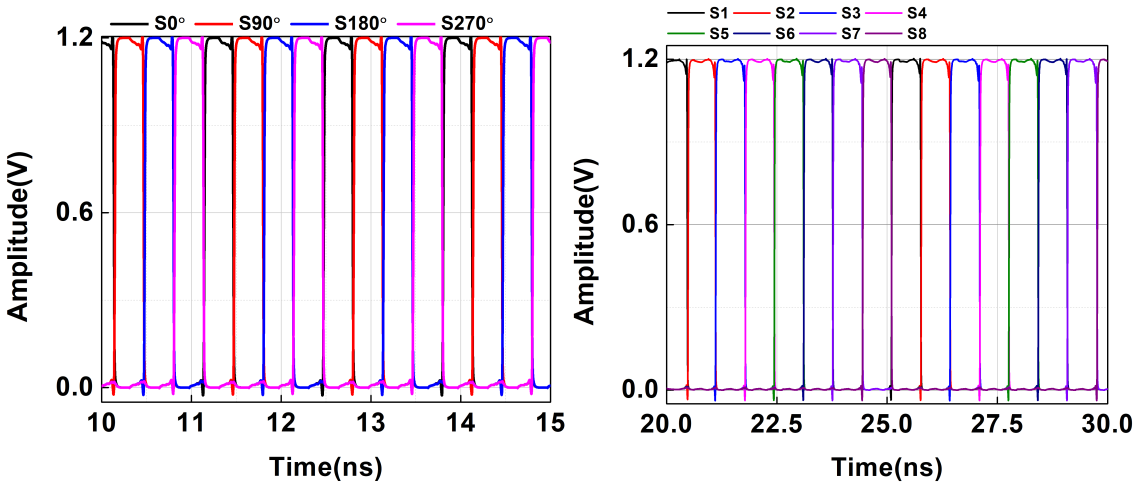
In addition, post-layout simulation of both the four and eight-phase non-overlapping clock generation circuits are also performed for an input signal frequency of 940 MHz. The four-phase and eight-phase outputs have 752 MHz, 188 MHz frequencies, respectively as shown in Fig. 4.9 (a) and Fig. 4.9 (b).



(a) (b)

Figure 4.8: (a) Transient IF outputs, (b) spectrum of the in-phase output

Similarly, the spectreRF simulations such as noise figure, input impedance, conversion gain and IIP_3 of the individual blocks of the proposed receiver RF front-end are performed.



(a) (b)

Figure 4.9: Post layout outputs of the (a) four phase and (b) eight-phase non-overlapping clock

The performance summary of the individual blocks of the process scalable architecture is given in Table. 4.1. The post-layout simulation for a f_{RF} of 940 MHz and f_s of 752 MHz shows that the noise figure, input impedance, gain and IIP_3 of the individual blocks are in agreement with the schematic simulation results.

Table 4.1: Post-layout performance summary of the proposed RF front-end

Parameter	Mixer	IF-LNA	IF Filter
Noise Figure(dB)	4	2	NA
Voltage Gain(dB)	-1.1	16	-0.7
IIP_3(dBm)	+16	-2.5	NA

4.2 Digitally Intensive Sub-Sampling Mixer-First Direct Down-Conversion RF Front-End

The proposed sub-sampling digitally intensive direct down-conversion receiver is implemented in 1.2 V, 65 nm CMOS technology, and it is a mixer-first sub-sampling receiver. As explained in Section 3.2, the RF front-end consists of an eight-path switch-capacitor sub-sampling quadrature down-conversion mixer, four BB-LNAs and eight g_m-cells at the BB-stage. Initially, the mixer translates the RF signal to base-band and the down-

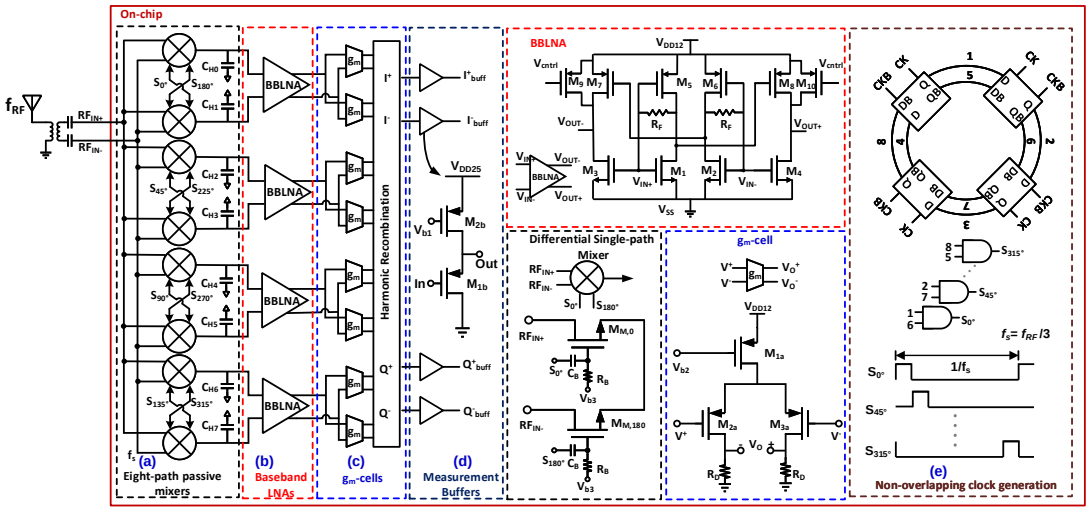


Figure 4.10: Different building blocks of the sub-sampling direct down-conversion receiver architecture and their circuit topologies: (a) eight-path passive mixer (b) BBLNA (c) g_m-cell (d) measurement buffer and (e) non-overlapping clocking scheme

converted outputs are given to four BB-LNAs. The outputs from these four BB-LNAs are combined using eight g_m cells to obtain IQ down-conversion using third harmonic of the f_s. The layout implementation details of individual blocks and the full chip layout of the proposed RF front-end, including the eight-phase non-overlapping clock generation circuits are provided. In addition, the post-layout performance of the RF front-end is also simulated and discussed in this section.

4.2.1 Circuit Implementation

This section explains the circuit-level implementations of the building blocks of the proposed RF front-end along with the non-overlapping clock generation scheme. The detailed circuit-level and block-level diagram of the proposed RF front-end is shown in Fig. 4.10

4.2.1.1 Eight-Path Switch-Capacitor Mixer

The differential eight-path passive mixer shown in Fig. 4.10(a) is employed in this work for down-conversion. The MOS switches are implemented with a minimum length of 60 nm, and the widths are chosen to have an on-resistance, R_{sw} of 10 Ω. Each switching

path is excited by one of the 12.5% duty cycle non-overlapping clock phases, S_{0° - S_{315° with quarter-rate sub-sampling frequency, f_s. Each path of the mixer conducts for $(\frac{1}{8})^{th}$ of the sampling period and samples the input RF signal onto hold capacitors, C_{H0} - C_{H7}. The eight outputs of the mixer are directly coupled to the input of the BBLNAs. The direct coupling of the mixer outputs to BBLNA forces the voltage at the source and the drain terminals of the mixer switches to the same gate voltage of the $M_{1,2}$ and $M_{5,6}$ of BBLNA. To accommodate this DC shift at the source and drain terminals of the switches the clock inputs are DC coupled with an additional biasing voltage V_{b3} at the gate terminal of the switches.

4.2.1.2 BBLNA

The circuit diagram of the CMOS inverter-based resistive feedback BBLNA is shown in Fig. 4.10(b). First-stage of the amplifier is designed to provide the required baseband impedance, given by Eq. (4.3), which is translated to RF port by the mixer to match 50 Ω.

$$R_{BB,LNA} = 2\left(\frac{R_F + R_o}{1 + G_m R_o}\right) \tag{4.3}$$

where $R_o = r_{o5,6} \| r_{o1,2}$ and $G_m = g_{m1,2} + g_{m5,6}$.

The second stage of the amplifier is designed to cancel the first-stage noise. The noise cancelling is achieved by matching the gain provided by second-stage NMOS ($M_{3,4}$) with the gain provided by CMOS inverter based resistive feedback first-stage together with second-stage PMOS ($M_{7,8}$). The total gain of the amplifier is given by Eq. (4.4), where R_F is the feedback resistor, and $A_v^{'} = \frac{1-G_m R_F}{1+\frac{R_F}{R_o}}$.

$$A_v = \left(A_v^{'} \times g_{m7,8} + g_{m3,4}\right)(r_{o3,4} \| r_{o7,8}) \tag{4.4}$$

The linearity of the BBLNA limits the mixer-first RF front-end linearity; hence, an auxiliary path with tuning option V_{cntrl} is provided to improve the linearity of the BBLNA, as shown in Fig. 4.10(b). For a tuning voltage, V_{cntrl} of 400 mV, the BBLNA provides an IIP_3 of -1 dBm. Therefore, increasing V_{cntrl} reduces the power consumption of the IF-LNA; however, as shown in Fig. 4.1, at low control voltages the linearity of the BB-LNA deteriorates the overall IIP_3 of the RF front-end.

4.2.1.3 Transconductance Amplifier

The circuit diagram of the PMOS-based transconductance amplifier (g_m-cell) is shown in Fig. 4.10(c). It is a PMOS differential amplifier with a resistive load that provides the second stage of amplification for the baseband signal. In the proposed eight-path operation, all the eight outputs are recombined with the uniform weighing gain of the g_m-cells to obtain quadrature outputs using the third harmonic down-conversion as shown in Fig. 3.3. The standalone g_m-cell offers a 6.5 dB voltage gain.

4.2.1.4 Measurement Buffer

The circuit diagram of the measurement buffer is shown in Fig. 4.10(d). The buffer is a common drain amplifier which is designed using 2.5 V supply transistors. It provides an IIP_3 of 32 dBm, -1.4 dB loss, a 50 Ω impedance at the output and consumes a 3 mW power. The buffer with such high linearity eliminates the need for de-embedding the buffer non-linearity in the measurements.

4.2.1.5 Non-overlapping Clock Generator

The eight-phase 12.5 % non-overlapping clocking scheme for the proposed RF front-end is shown in Fig. 4.10(e). An on-chip single-to-differential converter is employed to convert the external single-ended clock to a differential clock. These differential clock phases are divided by D-latch-based clock dividers, and the divider output phases are combined using combinational logic to generate non-overlapping clock phases with the required duty cycle.

4.2.2 Layout of the Individual Blocks

The proposed sub-sampling direct down-conversion receiver architecture is implemented in the 1.2 V, 65 nm CMOS technology and the full custom layout is implemented for the test chip. In this section, the post-layout performance summary of each block of the proposed RF front-end is presented.

4.2.2.1 Layout of the Eight-Path Mixer

The layout of the switch-capacitor direct down-conversion eight-path mixer is shown in Fig. 4.11. As explained in Section 4.2.1.1, the differential eight-phase mixer consists of eight differential switch stages and eight sampling capacitors. The differential RF inputs RF_{IN+}, RF_{IN-} are fed externally and non-overlapping clocks S_0 to S_7 are generated on the chip. The eight mixers are further connected to BB-LNAs for amplification and further processing.

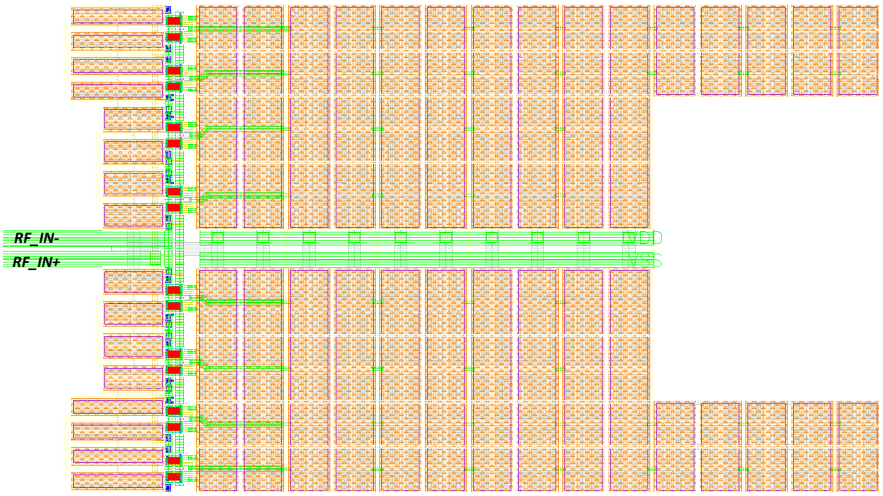


Figure 4.11: Layout of the eight-path mixer

4.2.2.2 Layout of the BBLNA

The layout of the CMOS inverter based resistive feed-back BB-LNA is shown in Fig. 4.12. The proposed receiver architecture has four BB-LNAs, the input to each of the LNA is applied at the LNA_{IN+}, LNA_{IN-} and the amplified base-band signal outputs are available at LNA_{OUT+} and LNA_{OUT-}. In this implementation, the BBLNAs are self-biased hence the decoupling capacitors are not required which reduces the area of the LNA.

4.2.2.3 Layout of the g_m-cell

The layout of the g_m-cell and measurement buffer is shown in Fig. 4.13. As shown in Fig. 4.10, the differential outputs of the BB-LNAs are combined using these g_m- cells to obtain IQ down conversion using the third harmonic of the f_s. The base-band buffers

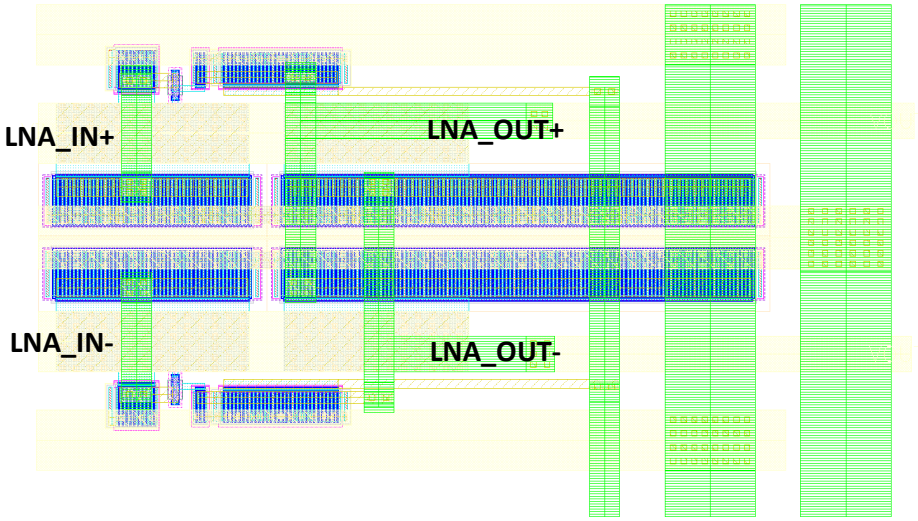


Figure 4.12: Layout of the BBLNA

are employed to buffer out the differential base-band IQ outputs I_{OUT+}, I_{OUT-}, Q_{OUT+} and Q_{OUT-}.

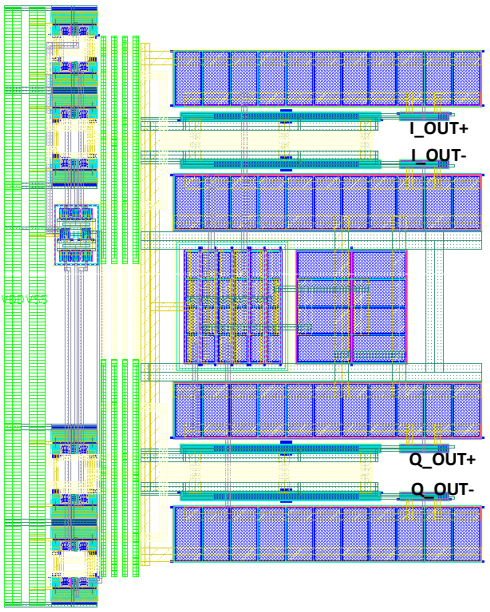


Figure 4.13: Layout of the g_m-cell and measurement buffer

4.2.2.4 Layout of the Eight-Phase Non-Overlapping Clock Generation

The switch-capacitor sub-sampling direct-down-conversion mixer requires eight non-overlapping clock generation circuits. The eight-phase non-overlapping circuit has two differential inputs CLK, CLK_{BAR} and eight non-overlapping phase outputs S_1 to S_7. The input to the eight-path clock generation circuit is provided externally. As explained in Section 4.2.1.5, an on-chip single-to-differential converter is employed to convert the external single-ended clock to a differential clock. The layout of the non-overlapping eight-phase clocking circuit is shown in Fig. 4.14.

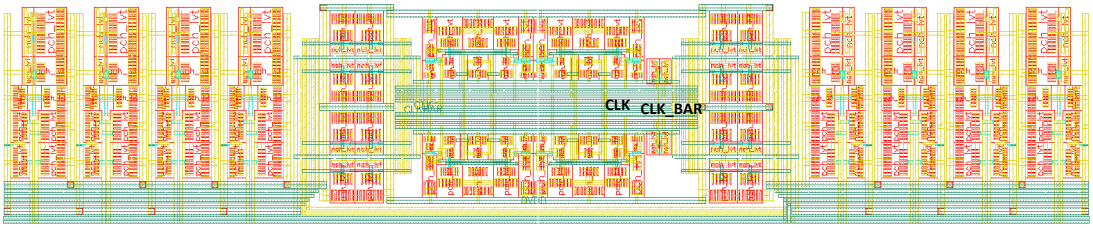


Figure 4.14: Layout of the eight-phase clock generation circuit

The full custom layout architecture of the proposed architecture is implemented, shown in Fig. 4.15.

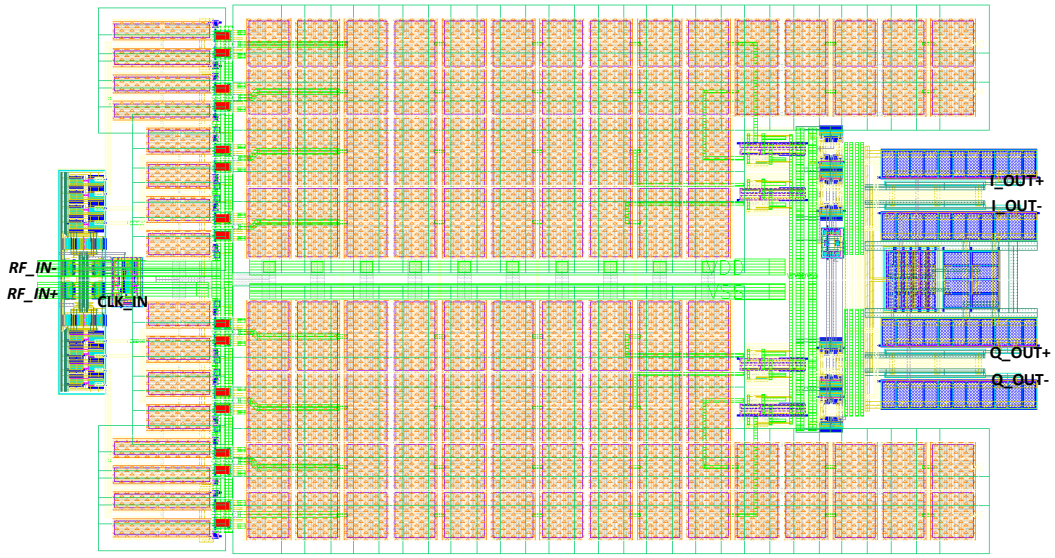


Figure 4.15: Layout of the full architecture

4.2.3 Post-Layout Performance

The post-layout performance of the proposed direct down-conversion receiver architecture is simulated, and the results are discussed. The transient and small signal performances of the proposed RF front-end are simulated. The transient response of the proposed RF front-end is simulated for an RF frequency of 1490 MHz and a sampling frequency of 490 MHz. The simulated time domain and frequency spectrum of the base-band outputs are shown in Fig. 4.16(a) and 4.16(b), respectively. The transient outputs shown in Fig. 4.16(a) are in quadrature, and the spectrum of the in-phase output shown in Fig. 4.16(b). This confirms the down-conversion to base-band frequency which is equal to $f_{RF} - 3f_S$. In addition, the post-layout simulation of the eight-phase non-overlapping clock generation circuit is performed for an input signal frequency of 1470 MHz. The eight-phase outputs have 490 MHz frequency, and the outputs are shown in Fig. 4.16(c).

Similarly, the spectre RF simulations such as noise figure, input impedance, gain and IIP_3 of the individual blocks of the receiver are performed. The performance summary of the individual blocks of the process scalable architecture is given in Table. 4.2. The post-layout simulation for a f_{RF} of 1470 MHz and f_s of 490 MHz, shows that the noise figure, input impedance, gain and IIP_3 of the individual blocks are in agreement with the schematic simulation results.

Table 4.2: Post-layout performance summary of the digitally intensive direct down-conversion receiver

Parameter	Mixer	BBLNA	g_m-cell
Noise Figure(dB)	+3.2*	+2.4	+10.5
Voltage Gain(dB)	+0.4	+16	+8
IIP_3(dBm)	+13.9	-1	+2.6

* NFDSB

4.3 Full-Chip Layout

The layout of the full-chip contains both the proposed RF front-ends as shown in Fig. 4.17. Initially, the individual blocks of architecture-I are highlighted. They are (1) a multi-path harmonic rejection mixer and four-phase non-overlapping clock generator,

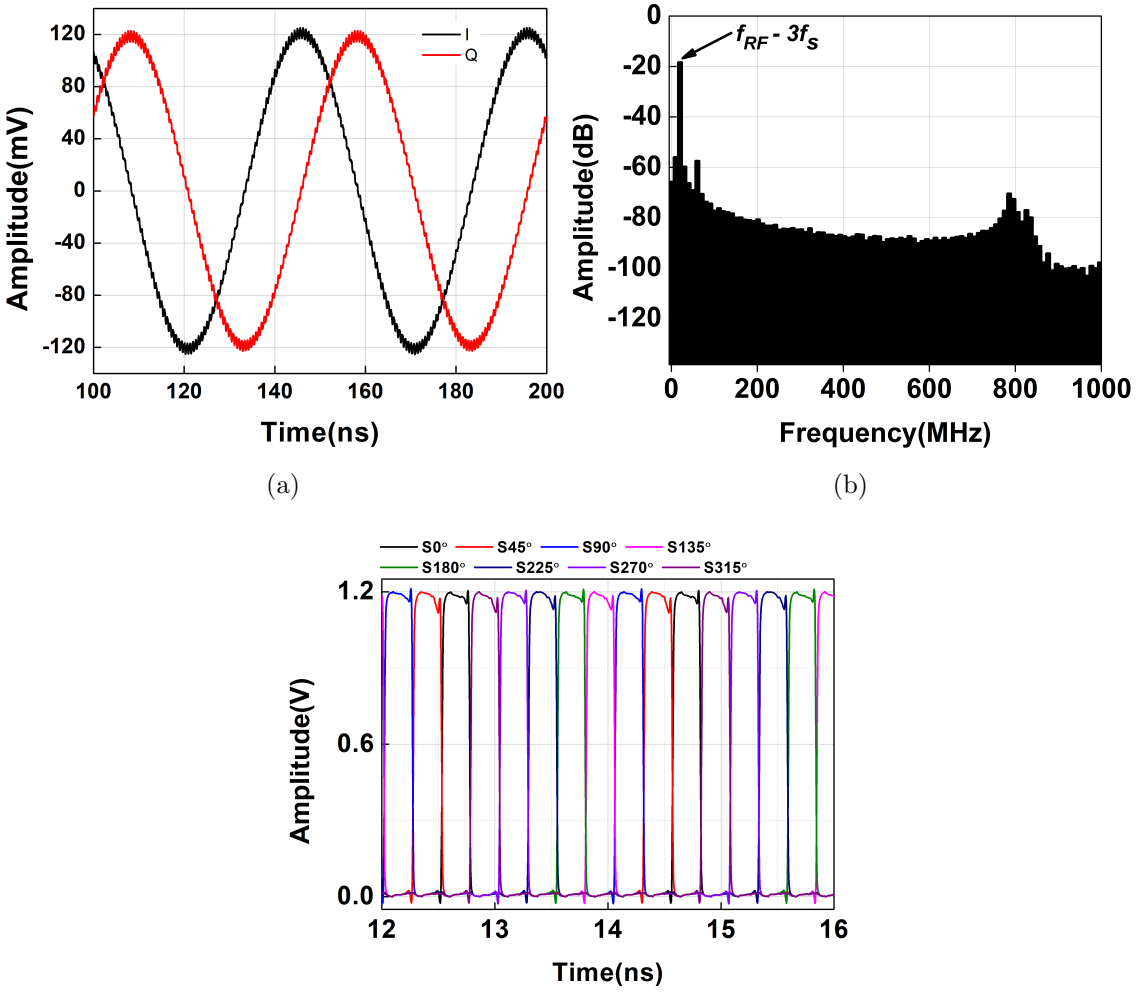


Figure 4.16: (a) Transient base-band outputs (b) spectrum of the in-phase output and (c) eight-phase non-overlapping clock

(2) an 8-phase non-overlapping clock generator circuit, (3) and (4) are M-phase complex impedance filter, (5) and (6) are IF-LNA stages and (7) and (8) are measurement buffers. The differential RF inputs RF_{IN+}, RF_{IN-} and clock input CLK_{in} for the architecture-I are fed at the bottom and the pins for the IF outputs IF_{I+}, IF_{I-}, IF_{Q+} and IF_{Q-} are also present at the bottom side the chip as shown in Fig. 4.17.

Similarly, the individual blocks of the architecture-II are highlighted. They are (1) sub-sampling zero-IF mixer and eight-phase non-overlapping clock generator, (2) base-band LNAs and g_m-cells and (3) measurement buffers. The differential RF inputs RF_{IN+}, RF_{IN-} and clock input CLK_{in} for the architecture-I are fed at the bottom and the pins for the base-band outputs BB_{I+}, BB_{I-}, BB_{Q+} and BB_{Q-} are also present at the upper

side the chip as shown in Fig. 4.17.

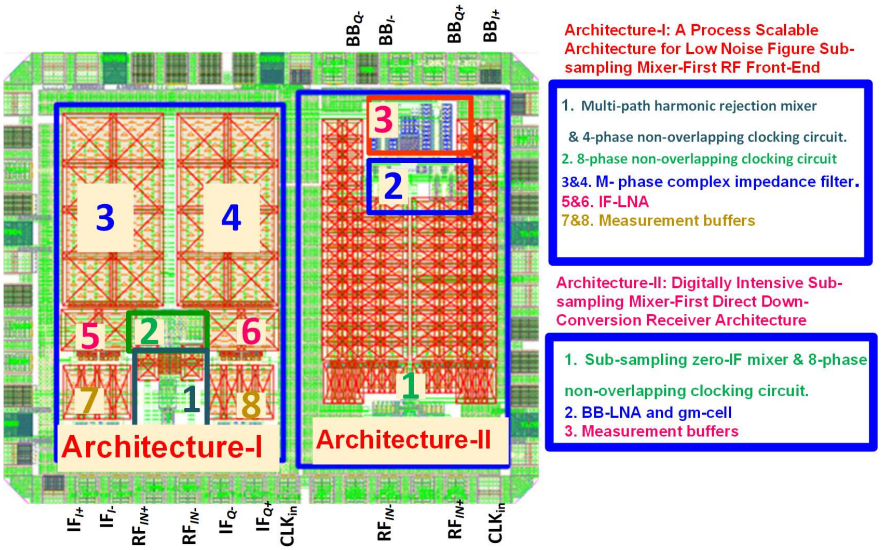


Figure 4.17: Layout of the full-chip

4.4 Conclusions

In this chapter, the circuit implementation details of both architectures are presented. The layout of each sub-system is developed and optimized to match the post-layout performance with the schematic simulations. At the end, the final layout of both the RF front-ends are implemented on single-chip, and the input-output is connected to a pad ring, shown in Fig. 4.17. The detailed measurement results of the test chip, containing both the proposed RF front-ends, are presented in Chapter 5.

Chapter 5

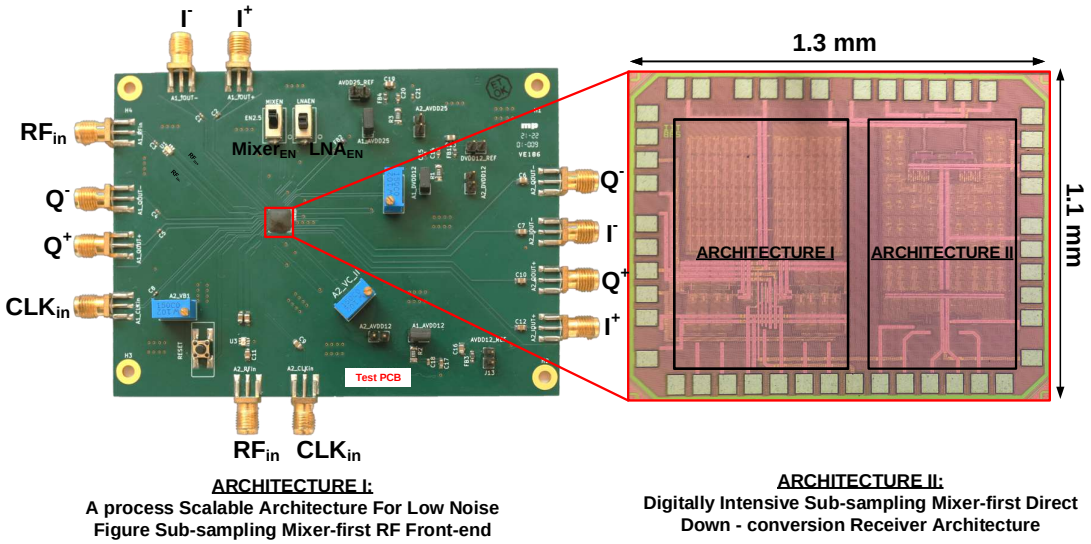
Measurement Results and Discussion

This chapter presents the details of the fabricated test chip, shown in Fig. 1.12 (a) of Chapter 1, PCB along with the test set-ups utilized to test and measure the performance of the two RF front-end architectures. Section 5.1 presents the measured performance of the first architecture, presented in Chapter 2, in terms of frequency spectrum down-conversion, harmonic rejection, conversion gain, impedance matching, linearity and input return loss. Similarly, Section 5.2 presents the measured performance of the second architecture, presented in Chapter 3. Section 5.3, the performance of the proposed RF front-ends compared with the state-of-the-art implementations individually and the summary of measurements is presented in Section 5.4.

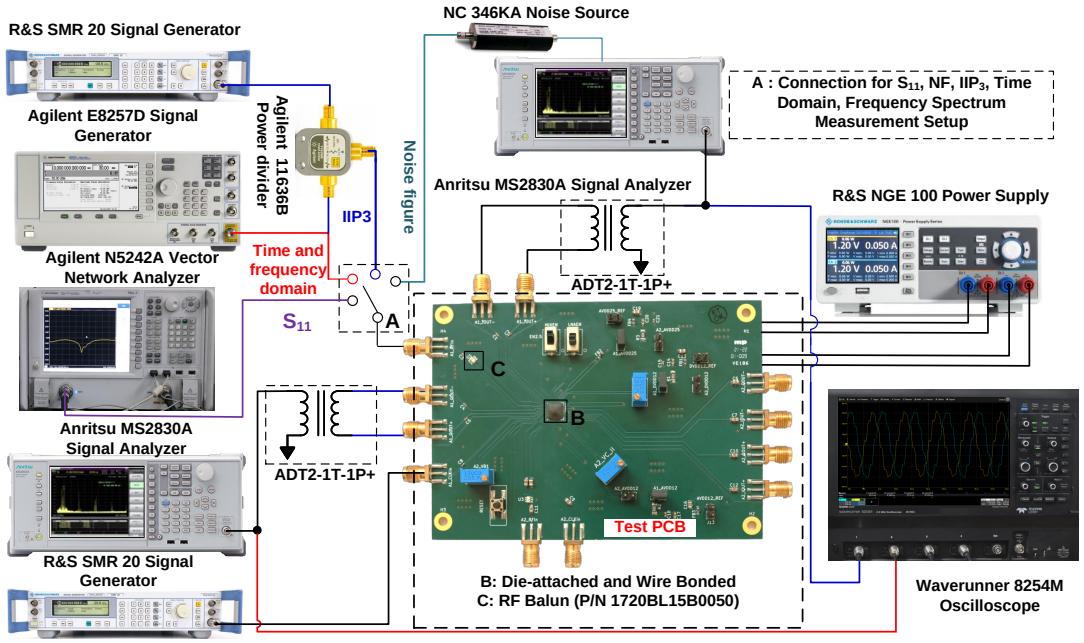
5.1 Process Scalable Architecture for Low Noise Figure Sub-Sampling Mixer-First RF Front-End

5.1.1 Measurement Setup

The proposed sub-sampling mixer-first RF front-end test chip is fabricated in 1P9M TSMC 65-nm CMOS technology. The RF front-end occupies an area of 0.33 mm^2. The micro-photograph of the test chip, along with the photograph of the PCB, are shown in Fig. 5.1(a). The test board is a four-layer FR4 PCB with coplanar RF and IF signal paths with 50 Ω line impedance. As shown in Fig. 5.1(a), the bare die is directly glued and wire bonded to the PCB. The test chip is powered by an external power supply of 1.2 V for the core analog/RF circuit and 2.5 V for measurement buffers. In addition, a 1.2 V digital supply for powering the on-chip non-overlapping clock generator circuit is used. This digital supply is separated from the analog/RF supply by a GND plane to decouple the switching noise. The commercial RF balun (P/N 1720BL15B0050) provides a wide-band operation from 400 MHz to 2815 MHz with a return loss of greater than 10 dB at the input and output ports and an insertion loss of less than 1 dB and the



(a)

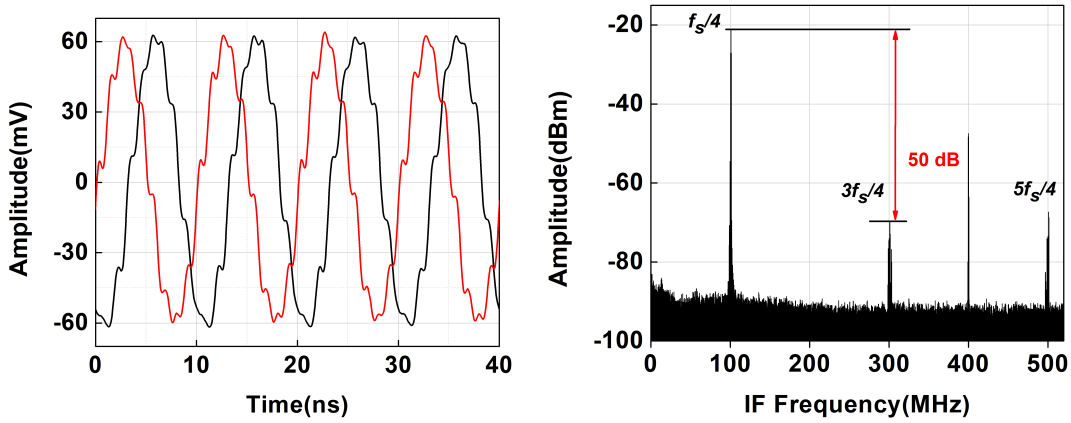


(b)

Figure 5.1: (a) Fabricated IC micro-photograph and the test PCB (b) measurement setup.

IF stage commercial off-chip balun (ADT2-1T-1P+) provides less than 0.8 dB insertion loss and greater than 20 dB return loss in the 8 MHz to 600 MHz frequency band. The losses of the RF balun, IF balun and connector cables are calibrated/de-embedded in the measurements except for input return loss measurements. The measurement setup is shown in Fig. 5.1(b), which includes test-chip, board, and measurement equipment.

An external clock and a single-ended RF input signal are applied from the left side of the PCB. Off-chip balun transformers are employed for the required single-ended to differential conversion. The balun and cable losses are de-embedded in the measurements except for linearity and input return loss measurements. Two external control signals LNA_{EN} and $Mixer_{EN}$ are available in the design to facilitate measurement of mixer output and mixer plus LNA output separately. The performance of the fabricated test chip is evaluated by carrying out various measurements such as the spectrum of frequency down-conversion, conversion gain, noise figure, linearity, and S_{11}. All the measurements are performed for the 0.4-1 GHz band of the standard IEEE 802.15.4, and elaborate measurements are done specifically for two bands centred at frequencies 860 MHz and 940 MHz.



(a) (b)

Figure 5.2: Measured (a) time domain output and corresponding frequency spectrum at IF for an f_{RF} of 501 MHz, and f_s of 400 MHz.

5.1.2 Quadrature Down-Conversion

The time-domain baseband quadrature outputs are measured for an f_{RF} of 501 MHz and f_s of 400 MHz. The four-path sub-sampling down-conversion mixer down-converted the input RF to 101 MHz as shown in Fig. 5.2(a). The measured quadrature outputs at the receiver output have an amplitude and phase mismatch of 1 mV and 5 degrees, respectively. The frequency spectrum of the in-phase output is measured for an f_{RF} of 500 MHz and f_s of 400 MHz. The frequency spectrum, Fig. 5.2(b) shows that the input RF down-conversion to 101 MHz and leakage of f_s at 400 MHz.

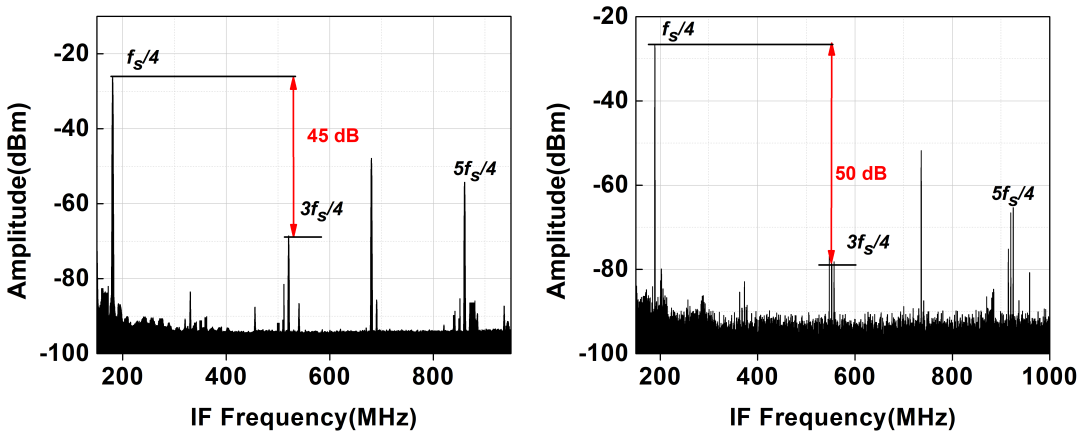


Figure 5.3: Measured frequency spectrum at IF (a) for an f_{RF} of 860 MHz, and f_s of 688 MHz, and (b) for an f_{RF} of 940 MHz, and f_s of 752 MHz.

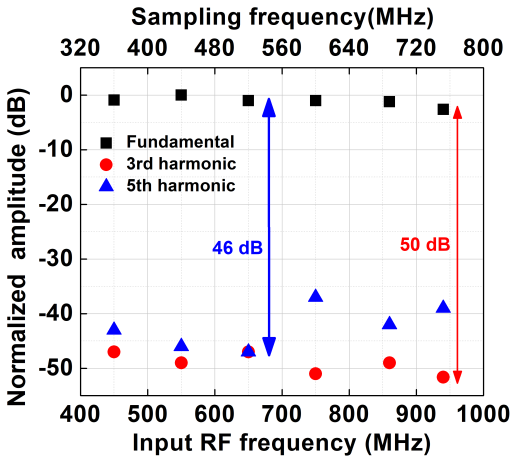


Figure 5.4: Measured IF harmonic rejection for varying input RF frequency and its corresponding sampling frequency.

5.1.3 Harmonic Rejection and Noise Figure

The measurement results of the proposed harmonic rejection scheme using the multi-path mixer are presented for the 0.4-1 GHz input RF range and the two specific 860 MHz and 940 MHz bands. For an input f_{RF} of 860 MHz and f_s of 680 MHz, the 4-path mixer translates the RF input to the $f_s/4$, $3f_s/4$ and $5f_s/4$, as shown in the frequency spectrum of Fig. 5.3(a). From these odd harmonics of $f_s/4$, the four-path mixer rejects the $3f_s/4$ and $5f_s/4$ harmonics by 48 dB and 41 dB, respectively. Similarly, as shown in frequency spectrum Fig. 5.3(b), for an input f_{RF} of 940 MHz and f_s of 752 MHz, the $3f_s/4$ and $5f_s/4$ harmonics are rejected by 50 dB and 36 dB, respectively. In addition, the measured

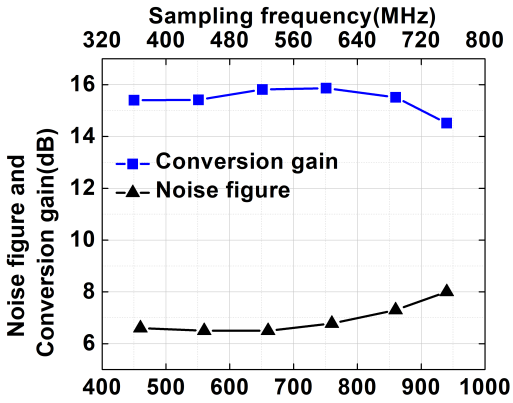


Figure 5.5: Measured noise figure and conversion gain with respect to input RF frequency and its corresponding sampling frequency.

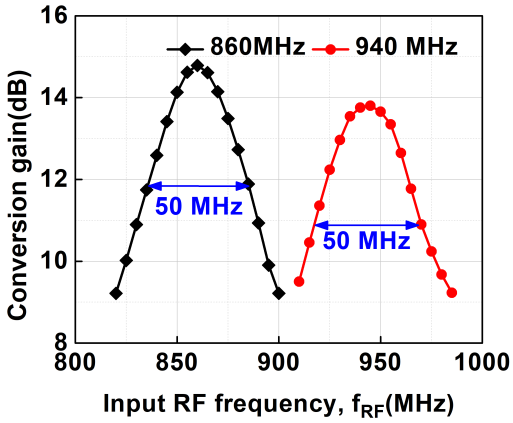


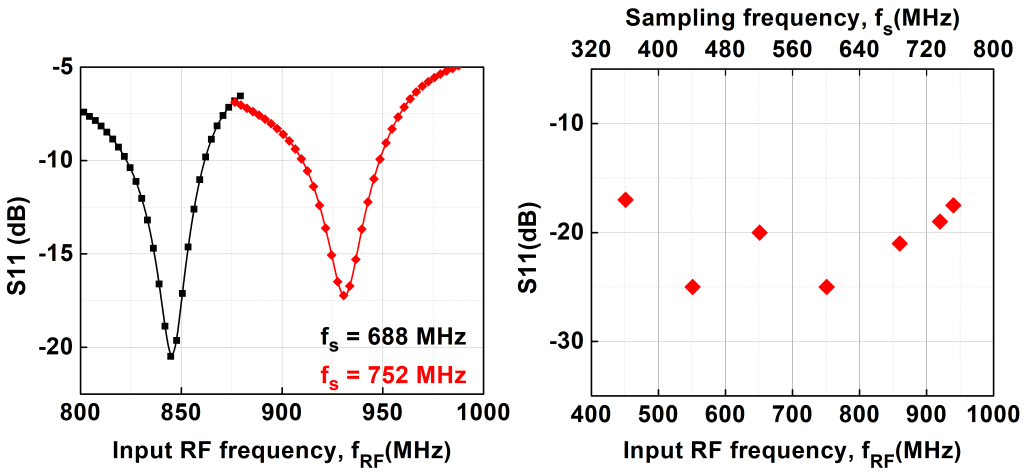
Figure 5.6: Measured conversion gain of the RF front-end for an f_{RF} of 860 MHz and 940 MHz.

harmonic rejection across the band from 0.4-1 GHz is shown in Fig. 5.4. The $3f_s/4$ and $5f_s/4$ harmonics are rejected by more than 46 dB and 36 dB, respectively, throughout the 0.4-1 GHz band.

These measured results confirm that the four-path mixer provides quadrature down-conversion and rejects the harmonic down-conversions to $3f_s/4$ and $5f_s/4$ for the selected sampling frequency for k = 2 as explained in the frequency plan in Section 2.2.2. The amplitude of the desired down-converted signal at $f_s/4$ is twice compared to a single-path mixer output. Hence, the measured noise figure of the 4-path harmonic rejection is only 4.5 dB when compared to the 7.5 dB noise figure of the single-path mixer noise.

The noise figure of the RF front-end is measured by varying the sampling frequency from 0.32-0.8 GHz for a corresponding RF frequency range from 0.4-1 GHz, shown in Fig.

5.5. The RF front-end that includes a multi-path mixer, IF-LNA, and IF filter has a noise figure of 6.5 dB for a conversion gain of 15.1 dB. The noise figure of the proposed RF front-end varies from 6.5 dB to 8 dB, which is 3.5 dB lower than the required noise figure calculated from the physical layer parameters of the IEEE 802.15.4 standard.



(a) (b)

Figure 5.7: (a) Measured S_{11} for an f_{RF} of 860 MHz and 940 MHz (b) Measured S_{11} with respect to input RF frequency and its corresponding sampling frequency.

5.1.4 Conversion Gain and Input Return Loss S_{11}

The measured gain of the IF-LNA is 15.7 dB, and it varies by 0.4 dB in the frequency range from 0.4-1 GHz. Similarly, the RF front-end that includes a multi-path mixer, IF-LNA, and filter has a measured gain of 15.1 dB, as shown in Fig. 5.5. The gain is 15.1 dB in the band 0.4-1 GHz with a variation of 1.3 dB. In addition, the conversion gain of the RF front-end is also measured by varying the input RF and keeping f_s constant for both the 860 MHz and 940 MHz bands. The RF front-end has a conversion gain of 14.8 and 13.8 dB for 860 MHz and 940 MHz bands, respectively, with a 50 MHz bandwidth as shown in Fig. 5.6.

As explained in Section 2.3 of Chapter 2, the impedance matching is achieved at the RF port of the mixer using the transparency of the passive mixer from IF to RF. The IF-stage impedance matching scheme facilitates a 50 Ω impedance matching at RF. To verify the matching, the input return loss S_{11} of the proposed RF front-end is measured for the 860 MHz and 940 MHz bands using one-port VNA measurements. As shown

in Fig. 5.7(a), the S_{11} is better than -10 dB for both bands. In addition, Fig. 5.7(b) shows the measured input return loss S_{11} for f_s in the range from 0.32-0.8 GHz and the corresponding RF frequency range from 0.4-1 GHz. The measured S_{11} is better than -10 dB and tunable with respect to the sampling frequency. These S_{11} results ensure that the proposed impedance matching scheme provides tunable 50 Ω impedance matching over the 0.4-1 GHz band. However, due to the parasitic capacitance at the mixer RF input, the S_{11} notch is shifted [12].

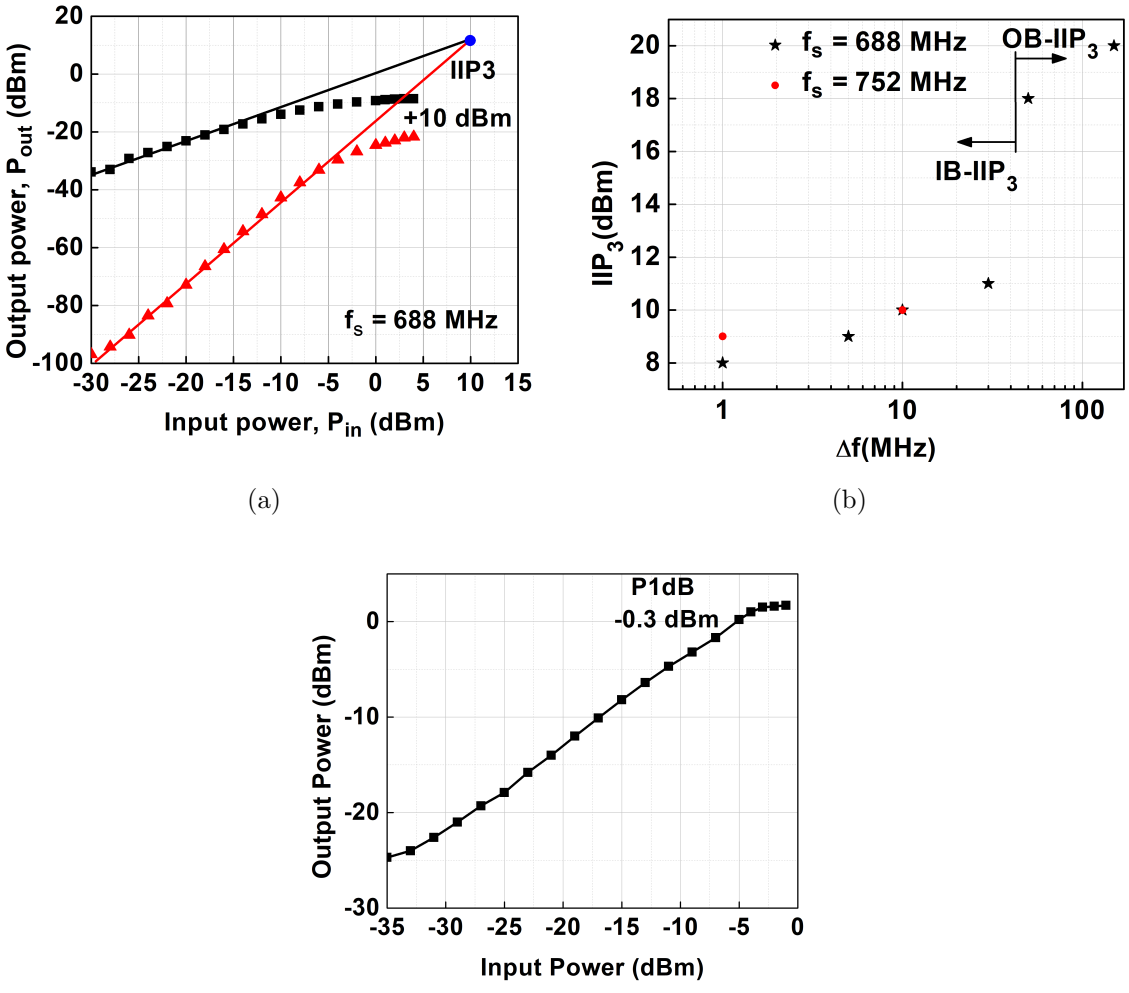


Figure 5.8: Measured IIP_3 (a) at an f_{RF} of 860 MHz, second tone is at a 10 MHz offset and (b) for varying Δf for both the 860 MHz and 940 MHz bands and (c) Measured P1 dB for an f_{RF} of 860 MHz and f_s of 688 MHz

5.1.5 IIP_3 and Power Consumption

IIP_3 of the RF front-end is measured by applying two tones, one tone at f_{RF} of 851 MHz, the other is at $f_{RF} + \Delta f$ = 861 MHz, for a sampling frequency, f_s of 688 MHz. The measured IIP_3 is +10 dBm for an offset of 10 MHz, shown in Fig. 5.8(a). Similarly, the IIP_3 of the RF front-end is measured for two specific bands with centre frequencies 860 MHz and 940 MHz for various frequency offsets(Δf), shown in Fig. 5.8(b). The RF front-end has a measured in-band IIP_3 of +18 dBm and +20 dBm out-of-band IIP_3. These results show that the proposed sub-sampling RF front-end maintains good linearity for both the in-band and out-of-band interferers. The P1dB performance of the proposed sub-sampling is investigated by performing compression test for an f_{RF} of 860 MHz and f_s of 688 MHz resulting in a P1dB of -0.3 dBm, shown in Fig. 5.8(c).

The switch-capacitor blocks of the RF front-end that includes a down-conversion mixer, and an IF stage M-phase filter together consume a power of 400 μW. This low power consumption makes the proposed sub-sampling mixer-first RF front-end suitable for low-power applications[53, 54] and is an alternative to RF sampling-based receivers[12]. As explained in section IV, the enhancement of IIP_3 performance has increased the IF-LNA power consumption. The measured power consumption of IF-LNA is 25 mW at V_c = 0.1 V. The non-overlapping clock generation and distribution for the 4-path mixer and 8-path filter consume 9.6 to 24 mW for an f_s of 0.32-0.8 GHz. The measurement buffer consumes a 3 mA current from the 2.5 V supply.

5.2 Digitally Intensive Sub-Sampling Mixer-First Direct Down-Conversion Receiver

5.2.1 Measurement Setup

The proposed quarter-rate sub-sampling direct down-conversion mixer-first RF front-end is implemented on the same test chip (shown in Fig. 1.12) and fabricated in 1P9M TSMC 65 nm CMOS technology. The RF front-end architecture occupies an active area of 0.32 mm^2. The test chip is directly attached to the test PCB using the chip on board (COB) method and wire bonded. The bare die is covered by epoxy to protect wire-bonded connections as shown in Fig. 5.1(a). The test PCB is a four-layer FR4 PCB with co-planar

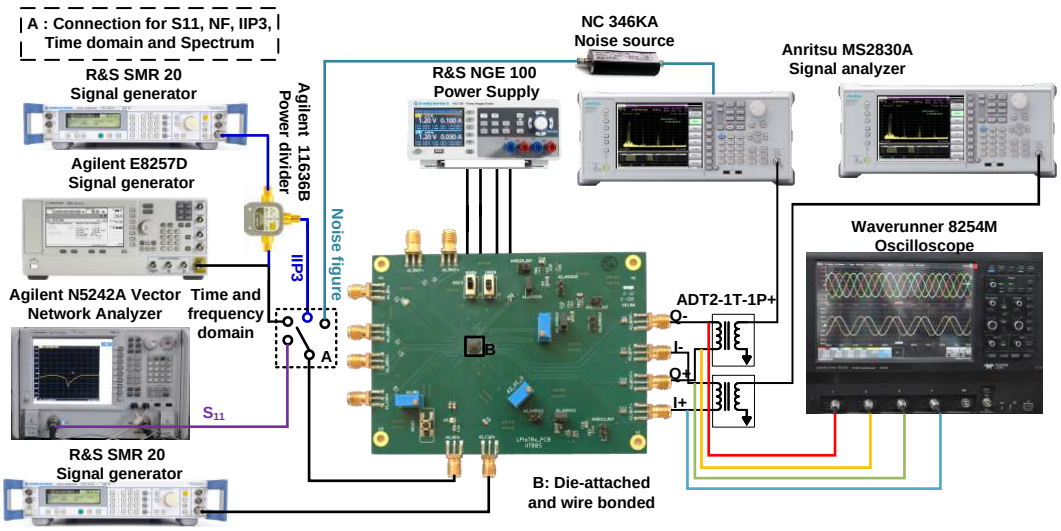


Figure 5.9: Measurement setup.

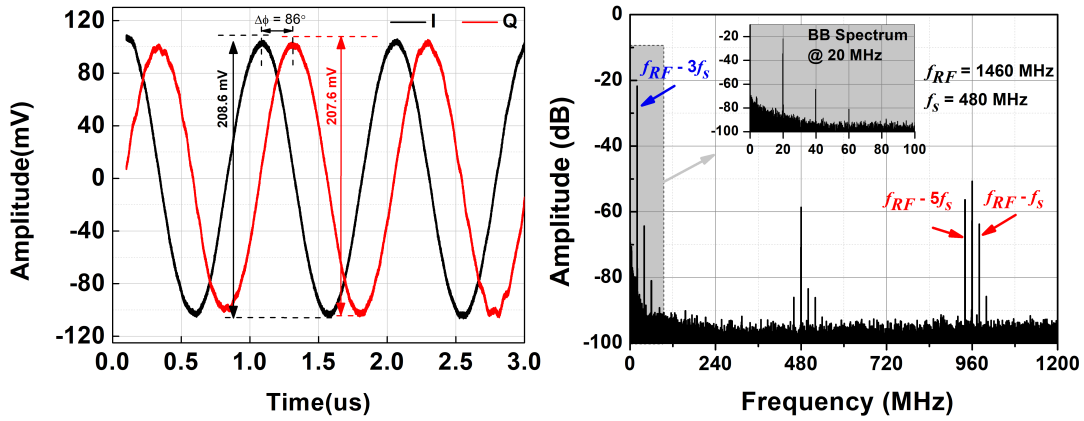
50 Ω RF baseband paths.

The block diagram of the measurement setup is shown in Fig. 5.9, along with the measurement equipment. The test chip is powered by an external supply of 1.2 V for core analog/RF and 2.5 V for the measurement buffers and I/O pads. A separate 1.2 V supply with a ground plane is used for powering digital sub-blocks to decouple the switching noise. Additionally, on-chip and off-chip decoupling capacitors are used to reduce the switching noise. Single-ended RF and clock inputs with 50 Ω are fed from the bottom side of the PCB. An off-chip balun transformer is mounted on PCB for the single-ended to the differential conversion of the RF input. Additionally, two external baluns are employed at the output for baseband differential to single-ended conversion. The balun and cable losses are de-embedded in the measurements except for the input return loss measurements. This section presents detailed measurement results of the proposed quarter-rate sub-sampling direct down-conversion RF front-end. All the measurements are performed for the 0.4-1.8 GHz, and detailed measurements are performed for an f_{RF} of 1.4 GHz.

5.2.2 Quadrature Down-Conversion

The time-domain baseband quadrature outputs are measured for an f_{RF} of 1462 MHz and f_s of 487 MHz. The eight-path sub-sampling down-conversion mixer down-converted the input RF to 1 MHz as shown in Fig. 5.10(a). The measured quadrature outputs

at the receiver output have an amplitude and phase mismatch of 1 mV and 6degree, respectively. The frequency spectrum of the in-phase output is measured for an f_{RF} of 1460 MHz and f_s of 480 MHz. The frequency spectrum, Fig. 5.10(b) shows the input RF down-conversion to 20 MHz and leakage of f_s at 480 MHz. This confirms the proposed quadrature sub-sampling direct down-conversion proposed in Section 3.2. In addition, the fundamental and fifth harmonic of f_s down-converting the f_{RF} of 1460 MHz to 940 MHz and 980 MHz, respectively, are attenuated by 36 dB, and 43 dB with respect to third harmonic down-conversion.

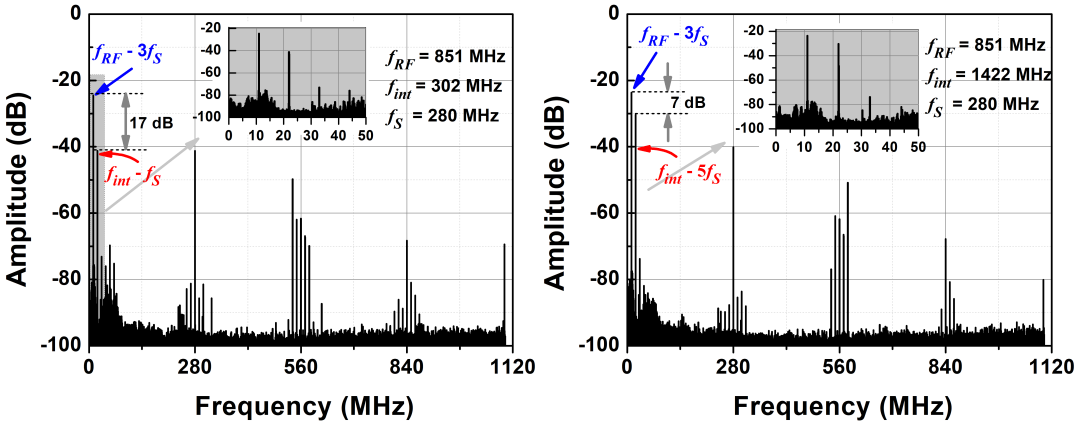


(a) (b)

Figure 5.10: Measured (a) transient base-band in-phase and quadrature outputs down-converted to 1 MHz for an f_{RF} of 1462 MHz and f_s of 487 MHz and (b) spectrum at the base-band for an f_{RF} of 1460 MHz and f_s of 480 MHz

In addition to the f_{RF} at $3f_s$, the mixer also translates the interferes present at the f_s and $5f_s$ to the baseband, with conversion gains as explained in Section 3.2.3, quantified by $\left|\frac{V_{I/Q,(1,5)}}{V_{I/Q,3}}\right|$ using the Eq. (3.5b), and (3.5c). To verify this, an RF signal is applied at the f_{RF} equals to $3f_s$ along with the interferer f_{int} at the f_s or $5f_s$ with the same amplitude. The measured baseband spectrum for the desired signal at, f_{RF} of 851 MHz, the interferer at, f_{int} of 302 MHz with an f_s of 280 MHz, translates to baseband with the desired signal located at 11 MHz and interferer located at 22 MHz as shown in Fig. 5.11(a). Similarly, Fig. 5.11(b) shows the frequency translations from the third and fifth harmonic of f_s to baseband for f_{RF} of 851 MHz and f_{int} of 1422 MHz to 11 MHz and 22 MHz respectively. These results show that the proposed harmonic recombination attenuates the down-conversion of the interferers at the fundamental and fifth harmonic of f_s by 17 dB and 7 dB respectively. Therefore, the proposed harmonic recombination provides an

additional harmonic rejection along with the RF filter for out of band harmonic blockers.



(a) (b)

Figure 5.11: Measured base-band output spectrum of the RF front-end for an f_s of 280 MHz and f_{RF} of 851 MHz in the presence of interferer, f_{int} at the (a) fundamental, and (b) fifth harmonic of f_s.

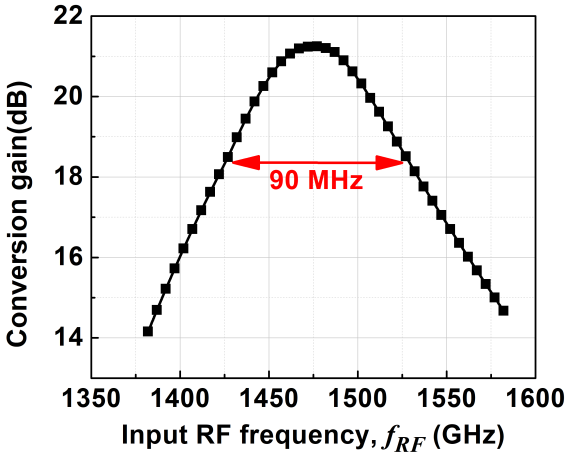


Figure 5.12: Measured conversion gain for an f_{RF} of 1470 MHz and f_s of 490 MHz

5.2.3 Conversion Gain and Noise Figure

The conversion gain of the sub-sampling direct down-conversion RF front-end is measured for an f_{RF} range of 0.4 GHz to 1.8 GHz by tuning the f_s from 0.13 GHz to 0.6 GHz. The RF front-end has a measured conversion gain of 22 dB with a maximum of 3 dB variation throughout the band, as shown in Fig. 5.13. To estimate the bandwidth, the conversion gain is measured by varying the f_{RF} around 1470 MHz, while keeping the f_s

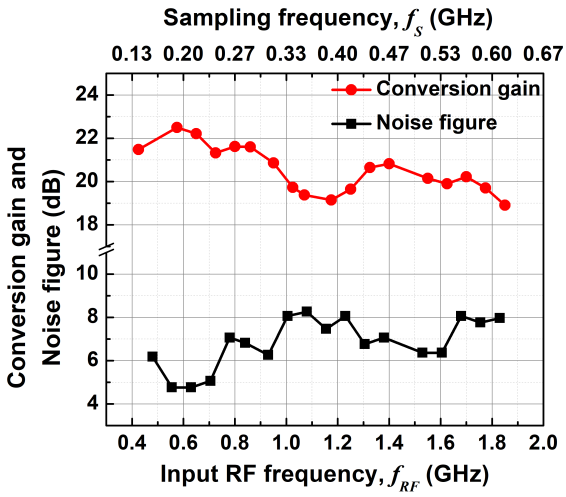


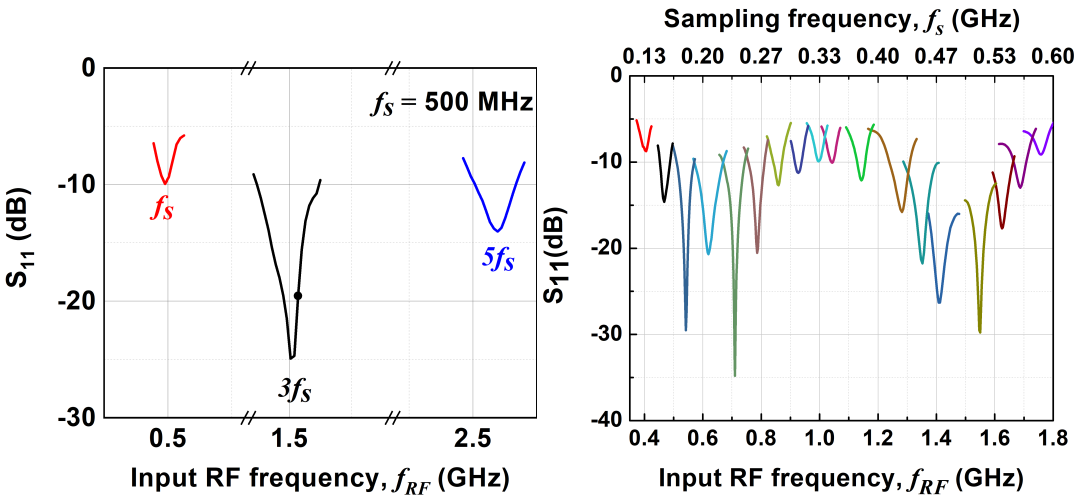
Figure 5.13: Measured conversion gain and noise figure with respect to input RF frequency, f_{RF} and its corresponding sampling frequency, f_s

at 490 MHz, shown in Fig. 5.12. The result shows that the RF front-end has a conversion gain of 21 dB at 1470 MHz with an estimated 3-dB bandwidth of 90 MHz.

The noise figure measurement setup of the sub-sampling direct down-conversion mixer-first RF front-end is shown in Fig. 5.1. The noise figure is measured for the input RF range of 0.4 GHz to 1.8 GHz. The measured DSB noise figure, shown in Fig. 5.13, is 4.7 dB for an f_{RF} of 0.6 GHz and f_s of 0.2 GHz, and as f_{RF} increased to 1.8 GHz, the noise figure is increased to 8 dB, due to lower conversion gain and return loss.

5.2.4 Input Return-Loss, S_{11}

The input impedance of the receiver is implemented by exploiting the transparency property of the passive mixer, as explained in Section 3.3. The switch-capacitor mixer translates the baseband impedance to the RF port of the mixer and is matched to 50 Ω at the third harmonic of f_s by tuning the input impedance of the base-band LNA. In the measurements, the input impedance matching is verified by one-port S_{11} measurements. Fig. 5.14(b) shows the S_{11} measured for an f_{RF} from 0.4 GHz to 1.8 GHz by varying the f_s from 0.13 GHz to 0.6 GHz. The measured S_{11} is better than -10 dB throughout the 0.4 GHz to 1.8 GHz frequency range. Similarly, to verify the impedance matching at desired third harmonic, and undesired fundamental and fifth harmonics of f_s, the S_{11} is measured for an f_s of 500 MHz and its corresponding harmonics. Fig. 5.14(a) shows the measured S_{11} is -25 dB at the $3f_s$, -10 dB at the f_s, and -12 dB at the $5f_s$. These results ensure



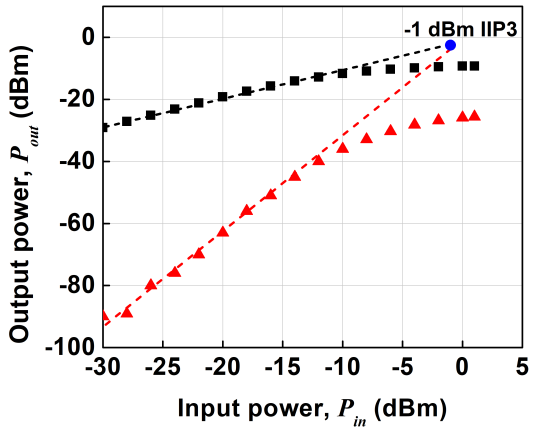
(a) (b)

Figure 5.14: (a) Measured S_{11} for an input RF frequency, f_{RF} of 1.5 GHz, sampling frequency, f_s of 500 MHz and (b) measured S_{11} with respect to f_{RF} and its corresponding f_s

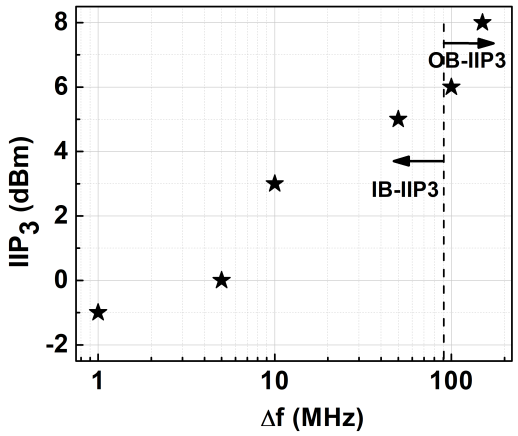
the proposed impedance matching scheme provides 50 Ω impedance to the RF port of the mixer using the third harmonic of f_s. The S_{11} notch is shifted from the centre frequency due to the capacitive parasitics, and this effect is increased as the f_{RF} is increased to 2 GHz.

5.2.5 IIP_3 and Power Consumption

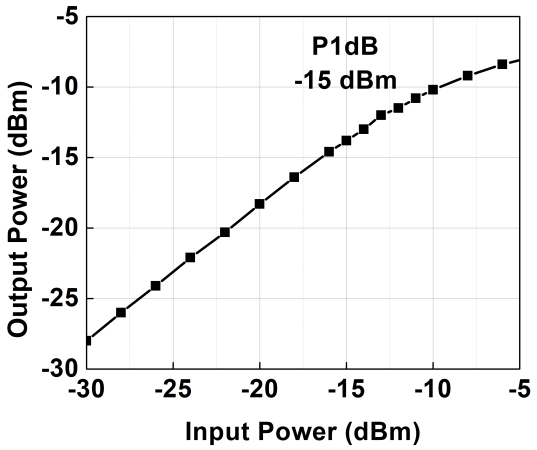
The IIP_3 of the sub-sampling direct down-conversion is measured by the two-tone test for an f_s of 490 MHz. Out of two tones, one tone is at f_{RF} of 1472 MHz, and another tone is with 1 MHz offset, i.e., at f_{RF} + Δf = 1473 MHz. Measured IIP_3 is -1 dBm as shown in Fig. 5.15(a). In addition, IIP_3 is measured for varying offset frequencies, Δf. The measured IIP_3 at an Δf of 45 MHz is +5 dBm; and for an out-of-band, Δf of 150 MHz is +8 dBm, shown in Fig. 5.15(b). These results show that the proposed quadrature sub-sampling direct down-conversion RF front-end maintains good linearity for both the in-band and out-of-band interferers over the input frequency range of 0.4-1.8 GHz. In addition, the P1dB performance of the proposed sub-sampling is investigated by performing compression test for an f_{RF} of 1470 MHz and f_s of 490 MHz resulting a P1dB of -15 dBm, shown in Fig. 5.15(c).



(a)



(b)



(c)

Figure 5.15: Measured IIP_3 (a) at an f_{RF} of 1472 MHz, with the second tone at 1 MHz offset and f_s of 490 MHz and (b) for varying Δf for an f_{RF} of 1460 MHz and (c) Measured P1 dB for an f_{RF} of 1472 MHz and f_s of 490 MHz

The switch-capacitor blocks of the RF front-end, 8-path down-conversion mixer consume the power of 800 μW. This low power consumption makes the proposed quarter-rate

sub-sampling mixer-first RF front-end is suitable for low-power applications. In addition, the enhancement of IIP_3 performance has increased the IF-LNA power consumption. The measured power consumption of IF-LNA is 23 mW at $V_c = 0.4$ V. The non-overlapping clock generation and distribution for the 8-path mixer consume 7.4 to 22 mW for an f_s of 0.13-0.6 GHz. The measurement buffer consumes 2.5 mW of power from the 2.5 V supply.

5.3 Performance Comparison

5.3.1 Process Scalable Architecture for Low Noise Figure Sub-Sampling Mixer-First RF Front-End

The performance comparison of the proposed RF front-end with the state-of-the-art sub-sampling and RF sampling receivers is presented in Table 5.1. The proposed sub-sampling RF front-end provides a re-configurable operation from 0.4-1 GHz for LR-WN applications. The RF front-end has a conversion gain of 15.1 dB and a noise figure of 6.5 dB, IIP_3 of +10 dBm. The proposed IF odd harmonic rejection multi-path mixer scheme alleviates the effect of noise folding, leading to a low-noise figure mixer. Hence, the proposed mixer-first RF front-end's noise figure becomes less than the LNA first sub-sampling down-conversion receivers[9, 26]. The IF-LNA, in combination with the switch-capacitor filter, offers the required impedance, and the impedance is frequency translated to f_{RF} by the transparency property of the passive mixer. Therefore, this is the first sub-sampling mixer-first RF front-end demonstrating the low noise figure and impedance matching for 0.4-1 GHz operation with a bandwidth of 50 MHz. The total power consumption of the switch-capacitor RF front-end blocks 4-path mixer and IF stage filter is 400 μW, which makes the proposed sub-sampling mixer-first RF front-end suitable for low-power applications[53, 54]. In addition, the proposed sub-sampling down-conversion scheme required a sampling frequency less than the input RF, significantly reducing the power consumption of the frequency synthesizer and non-overlapping clock generator and distribution circuit compared to the RF sampling-based counterparts.

5.3.2 Digitally Intensive Sub-Sampling Mixer-First Direct Down-Conversion Receiver Architecture

The performance comparison of the proposed quarter-rate sub-sampling direct down-conversion RF front-end with the state-of-the-art sub-sampling and RF sampling receivers

Table 5.1: Performance summary and comparison with the state of the art RF front-ends

	[20]	[13]	[21]	[12]	[53]	[54]	[25]	[9]		**This work**
Sampling Scheme	RF sampling						Sub-Sampling			
Architecture	Mixer-first						LNA-first			**Mixer-first**
Impedance matching w/o LNA	Yes	Yes	Yes	Yes	Yes^a	Yes^b	No	No		**Yes**
Supply(V)	1.2	1.2/2.5	1.2	1.2/1.6	0.8	0.7	1	1.2		**1.2**
Technology(nm)	65	65	28	40	22-SOI	65	28	65		**65**
f_{RF}(GHz)	0.2-2	0.1-2.4	0.2-2	0.1-0.7	0.6-1.3	2.3-2.5	58.2-64.8	2.4-2.483	4.5-5.7	**0.4-1**
f_s(MHz)	0.2-2	0.1-2.4	0.2-2	0.1-0.7	0.6-1.3	2.3-2.5	37.2-43.6	1.92-1.99	1.7-2.15	**0.32-0.8**
NF(dB)	9.5	6-8	7.3-10.6	9.8-12.7	8-9	9.5	7	11.5	12	**6.5**
BW(MHz)	25	20	18	3.2-4.8	16	NR	NR	20-77		**50**
IIP_3(dBm)	+11	25^c	33.3^c	24^c	25^c	-9.2	NR	-23 to -8	-21.5 to 8	**+10, +20**^{c}
Gain(dB)	19	40-70	13	40	13-14	20.6	36	26-40		**15.1**
HR3,5(dB)^d	NR	11 & 20	NA	>38/>35^e	NA	NA	NA	NA		**50, 46**
Power(mW) Mixer	NR	NR	NR	NR	0.6 ^{f}	0.194^g	204^h	NR	NR	**0.4**^{i}
Power(mW) LO	7-60	7.2-39.6	3-36	7-53		NR		NR	NR	**9.6 -24**^{j}
Power(mW) IF/BB	67	30	100,43	52	NR	NR		27.8	27.8	**25**
Area(mm^2)	0.13	0.75	0.48	2.03	0.23	0.45	NA	0.36	0.36	**0.32**

a: Passive network; b: On-chip inductor matching network; c: OOB-IIP_3; d:3rd and 5th harmonic rejection; e: HR w/o calibration; f: Excluding IF/BB power ; g: Excluding IF/BB and LO power; h: Estimated; i:Including IF-stage M-phase filter power consumption j: Power consumption including both 4-phase and 8-phase clocks; NF: Noise figure(SSB); BW: Bandwidth

Table 5.2: Performance summary and comparison with the state of the art RF front-ends

		[13]	[23]	[21]	[12]	[24]	[26]	[9]		**This work**
Sampling Scheme		RF sampling					Sub-Sampling			**Quarter-rate Sub-sampling**
Direct down-conversion		Yes	Yes	Yes	Yes	Yes	No	No		**Yes**
Architecture		Mixer-first				LNA-first	LNA-first			**Mixer-first**
Impedance matching w/o LNA		Yes	Yes	Yes	Yes	No	No	No		**Yes**
Supply(V)		1.2/2.5	1/1.2	1.2	1.2/1.6	1.5	0.6	1.2/2.5		1.2
Technology(nm)		65	28	28	40	130	65	65		65
f_{RF}(GHz)		0.1-2.4	0.1-2	0.2-2	0.1-0.7	0.8-4	2.4/2.7	2.4-2.483	4.5-5.7	**0.4-1.8**
f_s(GHz)		0.1-2.4	0.1-2	0.2-2	0.1-0.7	0.8-4	0.3	1.92-1.99	1.7-2.15	**0.13-0.6**
NF (dB)		4±1[a]	4.1-10.3[a]	4.3-7.6[a]	6.8-9.7[a]	3.8	6/5	12	11.5	**4.7-8**[a]
BW(MHz)		20	6.5	18	3.2-4.8	6/8	1	20-77		**90**
IIP_3(dBm)		25[b]	35[b]	33.3[b]	24[b]	-3.5[c]	NR	-23 to -8[c]	-21.5 to -8[c]	**-1**[c], +8[b]
Gain(dB)		40-70	16	13	40	28	40	26-41	26-38.5	22
Power(mW)	LO	7.2-39.6	34-96	3.6-36	7-53	33[d]	NR	NR	NR	7.4-22
	BB	30	30	100,43	52	NR	1.3	27.8	27.8	26[e]
Area(mm^2)		0.75	0.8	0.48	2.03	0.25	0.35	0.36	0.36	0.32

a: DSB noise figure; b: Out of band IIP_3; c: In-band IIP_3; d: Mixer and non-overlapping clock generation power consumption; e: Power consumption of BBLNA and g_m-cells

is presented in Table 5.2. The RF front-end provides a re-configurable operation from 0.4-

1.8 GHz using an f_s of 0.13-0.6 GHz. The measured noise figure of the RF front-end is 4.7 dB for a conversion gain of 22 dB, which is the lowest among the sub-sampling RF front-end architectures[9, 26]. In addition, the noise figure achieved by the proposed RF front-end is almost the same as RF sampling counterparts[12, 13, 21, 23] using a sampling frequency equal to one-third of RF sampling counterparts. The proposed impedance matching scheme using the harmonics of f_s eliminates the need for an additional matching network for sub-sampling RF front-ends[9, 26, 28]. Therefore, this is the first sub-sampling mixer-first RF direct down-conversion front-end demonstrating the direct down-conversion, low noise figure and impedance matching for 0.4-1.8 GHz operation with a bandwidth of 90 MHz and +8 dBm OB-IIP$_3$.

5.4 Conclusions

The measured performance of both the sub-sampling RF front-ends is presented. It is shown that, the sub-sampling facilitates implementing down-conversion using a sampling frequency less than input f_{RF}. In addition, it is also shown that the quarter-rate down-conversion scheme facilitates direct down-conversion using third harmonic of f_s. A proof-of-concept test chip is fabricated in 1.2 V, 65 nm CMOS to validate the proposed ideas. The measurement results show that the proposed sub-sampling down-conversion schemes are suitable candidates for implementing low-power re-configurable mixer-first RF front-ends.

Chapter 6

Summary, Conclusions and Future Work

6.1 Summary

This thesis deals with the development of a re-configurable switch-capacitor sub-sampling mixer-first RF front-ends for low-power wide-band applications. To date, sub-sampling has not been considered for mixer-first receivers due to high noise folding, non zero-IF down-conversion and difficulty in providing the impedance matching at the RF port. The proposed key contributions include architectural-level innovations such as a sub-sampling multi-path mixer harmonic rejection scheme, an IF-stage impedance matching scheme, and eight-phase harmonic recombination mixing scheme for achieving sub-sampling direct down-conversion along with the impedance matching at the RF port. In addition, the proposed circuit-level innovations include a multi-path sub-sampling mixer, M-phase switch-capacitor filter, inverter-based low noise amplifier to provide low noise figure, high linearity and most importantly, tunable IF stage impedance to match the RF port to a 50 Ω antenna impedance.

Based on the schemes discussed above, two sub-sampling mixer-first RF front-end architectures have been proposed to achieve low noise figure, 50 Ω impedance matching at the RF port, and high linearity while using a sampling frequency(f_s) less than input RF signal frequency(f_{RF}). The first architecture is a process scalable mixer-first RF front-end. The second architecture is a digitally intensive sub-sampling direct down-conversion mixer-first RF front-end. In this work, the circuit topologies of both the RF front-ends are implemented in 1.2 V, 65 nm technology and a test chip is fabricated.

Chapter 2 presents a process scalable architecture for low noise figure mixer-first RF front-end architecture based on sub-sampling down-conversion. The proposed RF front-end employs a switch-capacitor multi-path harmonic rejection mixer that rejects the harmonic down-conversions to odd multiples of $f_s/4$ such as $3f_s/4$, $5f_s/4$ to alleviate the effect of noise folding and leading to low noise figure sub-sampling mixer. The impedance

matching at the RF port of the mixer is achieved by the combination of the M-phase switch-capacitor filter and IF-LNA. The complete analysis of the sub-sampling frequency plan, amount of harmonic rejection, conversion gain, noise figure, linearity and the input impedance is presented. To validate the analysis and to explain the architecture, a sub-sampling RF front-end is implemented in 1.2 V, 65 nm CMOS and it is observed that the performance predicted by analytical equations is in agreement with spectreRF simulations. The proposed architecture is a digitally intensive RF front-end since the circuit components are process scalable switches, capacitors and inverters. In addition, a system-level error vector magnitude analysis for the proposed RF front-end architecture is presented.

The sub-sampling RF front-end presented in chapter 2 is a sub-sampling non zero-IF down-conversion RF front-end. Hence, a unique feature of sub-sampling is exploited to implement the first sub-sampling direct down-conversion RF front-end. Chapter 3 demonstrates the idea and implementation details of the sub-sampling direct down-conversion mixer-first RF front-end. The proposed RF front-end employs a quarter-rate sub-sampling scheme to implement direct down-conversion using sub-sampling and by exploiting the transparency property of the passive mixer impedance matching at the RF port by using harmonics of the sub-sampling frequency(f_s) and an eight-path mixer. In this work, the third harmonic of the f_s is employed to implement direct down-conversion to zero-IF. Hence, the proposed sub-sampling receiver architecture outperforms RF sampling receivers in terms of clock generation circuit power. The architecture is simulated, and the performance is verified using technology-scalable components like switches, capacitors, and inverters. It is observed that the proposed digitally intensive architecture performance predicted by analytical equations is in agreement with spectreRF simulations. In addition, a system-level error vector magnitude analysis of the proposed RF front-end architecture model is presented. Chapter 4 presents the CMOS implementation of individual blocks and complete RF front-ends, including the four-phase and eight-phase non-overlapping clock generation circuits. In addition, the optimized post-layout performance is also presented. The post-layout performance of the proposed digitally intensive architectures is in agreement with the schematic simulations. In chapter 5, a proof-of-concept 1.2 V, 65 nm CMOS test chip measurement results are presented along with the detailed analysis of the measured performance of both the proposed sub-sampling RF front-ends.

6.2 Conclusions

The proposed process scalable low noise figure sub-sampling mixer-first RF front-end addressed two major issues that are inherent to sub-sampling mixers, and they are high noise figure and lack of impedance matching. The proposed schemes are implemented at the circuit level by fabricating a test chip in 1.2 V, 65 nm CMOS technology covering the wide-band operation. The analytical equations, spectreRF simulations and measurement results established that the proposed sub-sampling mixer-first RF front-ends are suitable for low-power applications. The test chip measurement results show that it is possible to achieve low-noise figure, harmonic rejection, impedance-matching, high linearity, and reconfigurability along with low-power consumption, employing sub-sampling for implementing mixer-first RF front-ends. To the best of the author's knowledge, this is the first work reporting mixer-first RF front-ends in a sub-sampling paradigm.

The proposed digitally intensive sub-sampling mixer-first RF front-end employs a unique method of the quarter-rate sub-sampling direct down-conversion scheme along with RF port impedance matching. A proof-of-concept test chip is fabricated in 1.2 V, 65 nm CMOS to validate the proposed ideas. The measurement results show that the proposed sub-sampling down-conversion scheme is a suitable candidate for implementing low-power re-configurable mixer-first RF front-ends.

6.3 Future Work

Process scalability, circuit and architectural level innovations are the main factors driving improvements in RF receivers. With the advancements in CMOS technology, switch-capacitor circuits offer high linearity and improved switching speed. Owing to these advantages, the two digitally intensive sub-sampling mixer-first RF front-ends proposed in this thesis offer high linearity and programmable wide-band operation. However, the linearity of the proposed RF front-end depends on the linearity of IF or BBLNA. Hence, the performance of the IF-LNA is optimised to provide an IIP_3 greater than -2.5 dBm, which resulted in high power consumption. In future work, it is required to optimize the power consumption of the IF-LNA and BBLNA. Further, a new LNA topology with high linearity, gain, and low noise figure while consuming low power can be proposed. In this work, the proposed digitally intensive sub-sampling RF front-end employed a divider-based

N-phase non-overlapping generation scheme. This circuit requires a sampling frequency of at least $Nf_s/2$ to generate a non-overlapping clock of frequency f_s. On the other hand, in the future, a delay-based divider-less non-overlapping clock generator needs to be integrated with a sub-sampling RF front-end to reduce the power consumption further. Another obstacle in the implementation of sub-sampling mixer-first RF front-end using a sampling frequency less than the input RF signal is providing impedance matching; part of this issue is addressed in this work in Chapter 2 and Chapter 3. However, these techniques can be further extended to provide impedance matching at higher harmonics of f_s (beyond the third harmonic of f_s) to achieve very low power consumption.

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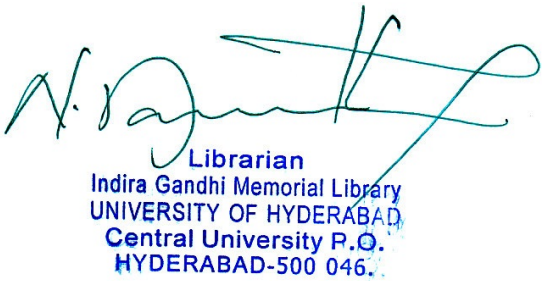

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